

PRELIMINARY

**NEC** NEC LCD Technologies, Ltd.

# TFT COLOR LCD MODULE

## NL192120BC25-03

**57cm (22.5 Type)**

**WUXGA**

**LVDS Interface (4 ports)**

## PRELIMINARY DATA SHEET

DOD-PP-0543 (2nd edition)



**This PRELIMINARY DATA SHEET is updated document from DOD-PP-0407(1).**

**All information is subject to change without notice. Please confirm the sales representative before starting to design your system.**

## INTRODUCTION

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Examples: Computers, office automation equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment, industrial robots, etc.

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Examples: Control systems for transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, medical equipment not specifically designed for life support, safety equipment, etc.

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Examples: Military systems, aircraft control equipment, aerospace equipment, nuclear reactor control systems, medical equipment/devices/systems for life support, etc.

The quality grade of this product is the "**Standard**" unless otherwise specified in this document.

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## 1. OUTLINE

### 1.1 STRUCTURE AND PRINCIPLE

Color LCD module NL192120BC25-03 are composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight. 2

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Grayscale data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

### 1.2 APPLICATION

- Color monitor system

### 1.3 FEATURES

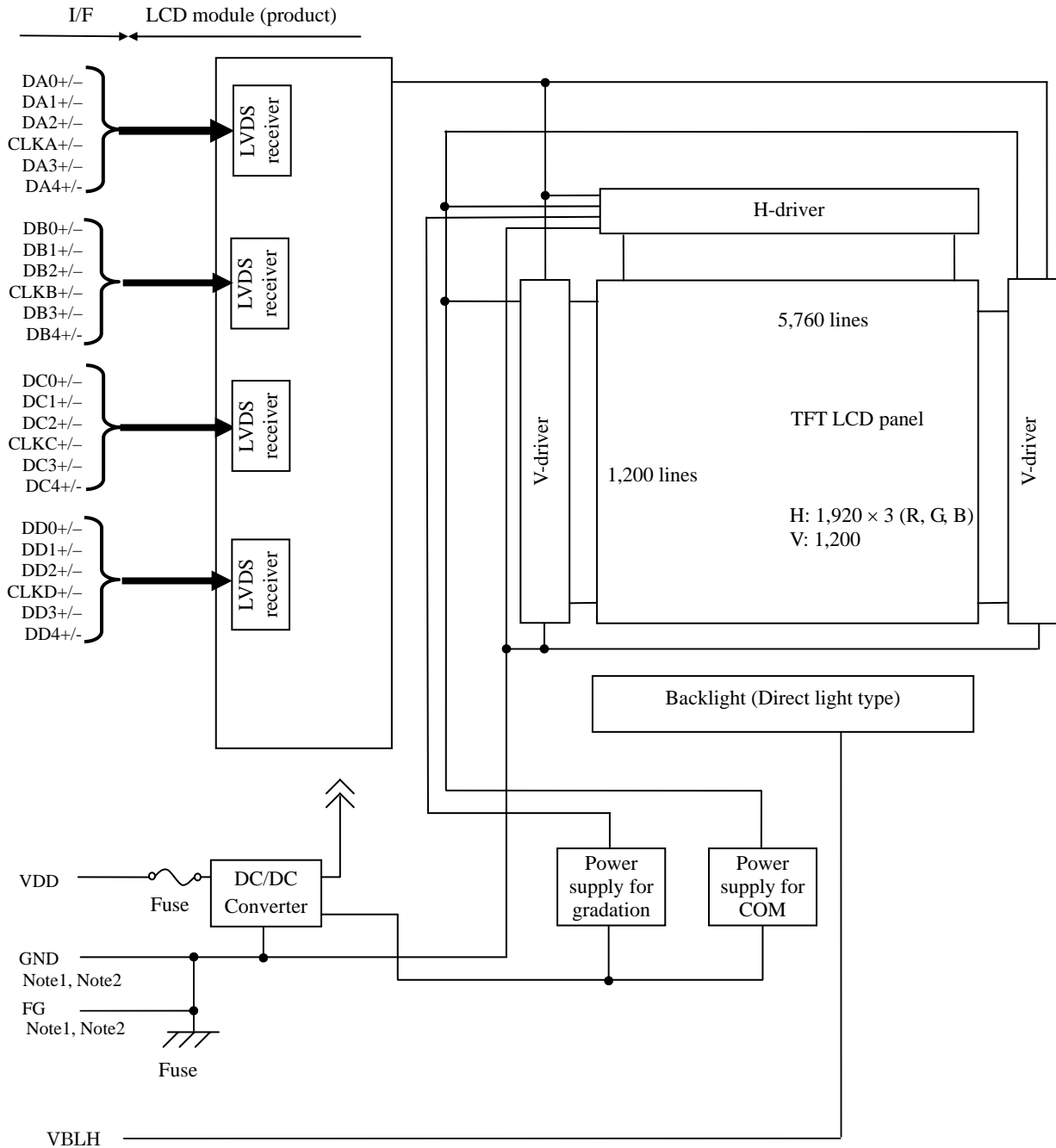
- Ultra-wide viewing angle (Adoption of Ultra-Advanced Super Fine TFT (UA-SFT))
  - Active matrix LCD
  - LVDS interface (4ports)
  - 1,024 gray scales per 1 sub-pixel (10-bit)
  - High contrast
  - 120Hz frame driving
  - Fast response time
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## 2. GENERAL SPECIFICATIONS

<b>Display area</b>	483.84 (H) × 302.4(V) mm	
<b>Diagonal size of display</b>	57.0 cm (22.5 inches)	
<b>Drive system</b>	a-Si TFT active matrix	
<b>Display gray scale</b>	1,073,741,824 colors (10-bit)	
<b>Pixel</b>	1,920 (H) × 1,200 (V) pixels	
<b>Pixel arrangement</b>	RGB (Red dot, Green dot, Blue dot) vertical stripe	
<b>Sub-pixel pitch</b>	0.084 (H) × 0.252 (V) mm	
<b>Pixel pitch</b>	0.252 (H) × 0.252 (V) mm	
<b>Module size</b>	542 (W) × 362 (H) × 40 (D) mm (typ.)/ 55.5 (D) mm (max.)	
<b>Weight</b>	(3,300) g (typ.)	2
<b>Contrast ratio</b>	(800:1) (typ.)	
<b>Viewing angle</b>	At the contrast ratio $\geq 10:1$ <ul style="list-style-type: none"> <li>• Horizontal: Right side 88° (typ.), Left side 88° (typ.)</li> <li>• Vertical: Up side 88° (typ.), Down side 88° (typ.)</li> </ul>	2
<b>Designed viewing direction</b>	Viewing angle with optimum grayscale ( $\gamma \approx 2.2$ ): normal axis (perpendicular)	2
<b>Polarizer surface</b>	Antiglare	
<b>Polarizer pencil-hardness</b>	2H (min.) [by JIS K5400]	
<b>Response time</b>	$T_{on} + T_{off}$ (10% ← → 90%) (12) ms (typ.)	
<b>Luminance</b>	At IBL = (5.0) mA rms (500) cd/m <sup>2</sup> (typ.)	2
<b>Color gamut</b>	At LCD panel center (77) % (typ.) [against NTSC color space]	
<b>Signal system</b>	4 ports LVDS interface (THC63LVD104S×2pcs, THine Electronics, Inc. or equivalent) [RGB 10-bit signals, Data enable signal (DE), Dot clock (CLK)]	2
<b>Power supply voltage</b>	LCD panel signal processing board: 12.0V	
<b>Backlight</b>	Direct light type: 12 cold cathode fluorescent lamps (without an inverter)	
<b>Power consumption</b>	TBD W (typ.)	

### 3. BLOCK DIAGRAM



Note1: Relations between GND (Signal ground) and FG (Frame ground) in the LCD module are as follows.

GND - FG	Connected
----------	-----------

Note2: GND and FG must be connected to customer equipment's ground, and it is recommended that these grounds are connected together in customer equipment.

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## 4. DETAILED SPECIFICATIONS

### 4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	542 ±0.5 (W) × 362 ±0.5 (H) × 40 ±0.5 (D) 55.5 (max., D)	Note1 mm
Display area	483.84(H) × 302.4 (V)	Note1 mm
Weight	(3,300) (typ.)	g

Note1: See "7. OUTLINE DRAWINGS".

2

### 4.2 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board	VDD	-0.3 to +14.0	V	Ta=25°C
	Lamp voltage	VBLH	TBD	Vrms	
Input voltage for signals	LVDS signal Note1	VD	-0.3 to+2.6	V	Ta=25°C VDD = 12.0V
Storage temperature		Tst	(-20 to +60)	°C	-
Operating temperature	Front surface	TopF	(0 to +50)	°C	Note2
	Rear surface	TopR	TBD	°C	Note3
Relative humidity Note4		RH	≤ 95	%	Ta ≤ 40°C
			≤ 85	%	40°C < Ta ≤ 50°C
Absolute humidity Note4		AH	≤ 70 Note5	g/m <sup>3</sup>	Ta > 50°C

Note1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CLKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CLKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CLKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CLKD+/-

Note2: Measured at center of LCD panel surface (including self-heat)

Note3: Measured at center of LCD module's rear shield surface (including self-heat)

Note4: No condensation

Note5: Water amount at Ta = 50°C and RH = 85%

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## 4.3 ELECTRICAL CHARACTERISTICS

### 4.3.1 LCD panel signal processing board

(Ta= 25°C)

Parameter	Symbol	min.	typ.	max.	Unit	Remarks	
Power supply voltage	VDD	10.8	12.0	13.2	V	-	
Power supply current	IDD	-	(1,000) Note1	(1,800) Note2	mA	at VDD = 12.0V	
Permissible ripple voltage	VRP	-	-	100	mVp-p	for VDD	
Differential input threshold voltage for Display signals	High	VTH	-	-	+100	mV	at VCM= 1.2V Note3, Note4
	Low	VTL	-100	-	-	mV	
Input voltage swing	VI	0	-	2.4	V	Note4	
Terminating resistance	RT	-	100	-	Ω	-	

Note1: Checkered flag pattern [by EIAJ ED-2522]

Note2: Pattern for maximum current

Note3: Common mode voltage for LVDS receiver

Note4: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CKD+/-

2

2

### 4.3.2 Backlight lamp

(Ta= 25°C)

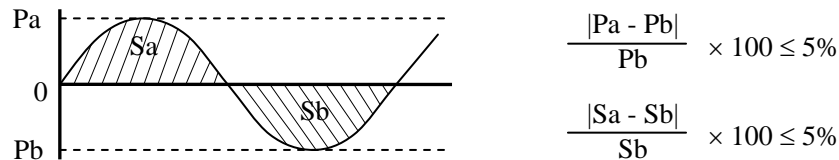
Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Lamp current	IBL	TBD	(5.0)	TBD	mArms	at IBL= (5.0) mArms: L= (500) cd/m <sup>2</sup> Note3, Note4
Lamp voltage	VBLH	-	(920)	-	Vrms	Note2, Note3
Lamp starting voltage	VS	TBD	-	-	Vrms	Ta= 25°C Note2, Note3, Note5
		TBD	-	-	Vrms	Ta= -20°C Note2, Note3, Note5
Lamp oscillation frequency	FO	TBD	(60)	TBD	kHz	Note6

2

Note1: This product consists of 12 backlight lamps, and these specifications are for each lamp.

Note2: The lamp voltage cycle between lamps should be kept on a same phase. "VS" and "VBLH" are the voltage value between low voltage side (Cold) and high voltage side (Hot).

Note3: The asymmetric ratio of working waveform for lamps (Power supply voltage peak ratio, power supply current peak ratio and waveform space ratio) should be less than 5 % (See the following figure.). If the waveform is asymmetric, DC (Direct current) element apply into the lamp. In this case, a lamp lifetime may be shortened, because a distribution of a lamp enclosure substance inclines toward one side between low voltage terminal (Cold terminal) and high voltage terminal (Hot terminal). When designing the inverter, evaluate asymmetric of lamp working waveform sufficiently.



Pa: Supply voltage/current peak for positive, Pb: Supply voltage/current peak for negative  
Sa: Waveform space for positive part, Sb: Waveform space for negative part.

Note4: This product consists of 12 lamps. The lamp current should be measured by high-frequency current meter at the low voltage terminal.

Note5: The inverter should be designed so that the lamp starting voltage can be maintained for more than 1 second. Otherwise the lamp may not be turned on.

Note6: In case "FO" is not the recommended value, beat noise may display on the screen, because of interference between "FO" and "1/th". Recommended value of "FO" is as following.

$$FO = \frac{1}{4} \times \frac{1}{th} \times (2n-1)$$

th: Horizontal cycle (See "4.8.1 Timing characteristics".)

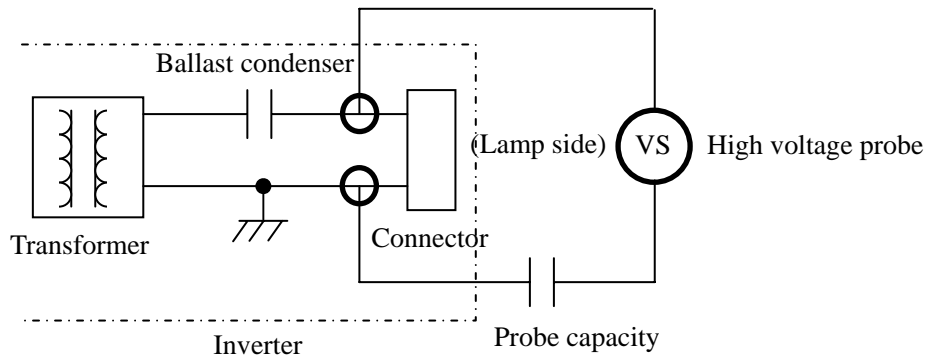
n : Natural number (1, 2, 3 .....)

Note7: Method of lamp cable installation may invite fluctuation of lamp current and voltage or asymmetric of lamp working waveform. When designing method of lamp cable installation, evaluate the fluctuation of lamp current, voltage and working waveform sufficiently.

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Note8: In case of Inverter with Ballast condenser, "VS" is the voltage level between Ballast condenser and Connector (Refer to the below "Example of measurement"). "VS" should be designed to be more than minimum "VS". Otherwise the lamp may not be turned on because the lamp starting voltage is less than minimum "VS".

Example of measurement  
Probe capacity: 3pF (Tektronix, inc.: P6015A)



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### 4.3.3 Power supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage (Measure at input terminal of power supply)	Note1	Unit
VDD	12.0 V	≤ 100		mVp-p

Note1: The permissible ripple voltage includes spike noise.

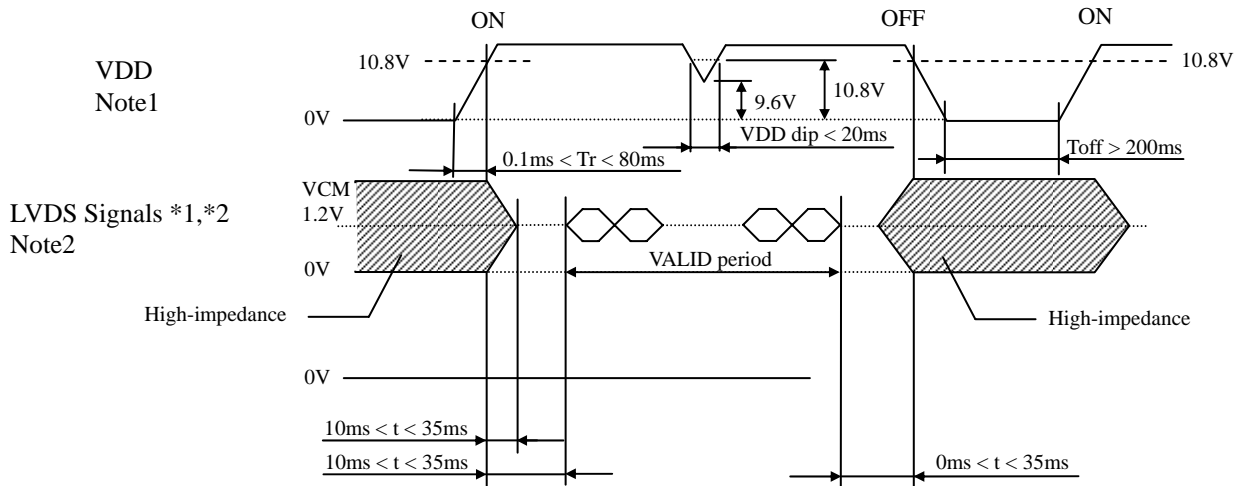
### 4.3.4 Fuse

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	TBD	TBD	TBD[A]	TBD[A]	Note1
			TBD[V]		

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

## 4.4 POWER SUPPLY VOLTAGE SEQUENCE

### 4.4.1 LCD panel signal processing board



- \*1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CLKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CLKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CLKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CLKD+/-
- \*2: LVDS signals should be measured at the terminal of 100Ω resistance.

- Note1: In terms of voltage variation (voltage drop) while VDD rising edge is below 10.8V, a protection circuit may work, and then this product may not work.
- Note2: LVDS signals must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged.  
If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. VDD should be cut when the display and function signals are stopped.
- Note3: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.

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## 4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

### 4.5.1 LCD panel signal processing board

CN1 socket (LCD module side): FI-RE51S-HF (Japan Aviation Electronics Industry Limited (JAE))  
 Adaptable plug: FI-RE51HL,FI-RE51CL (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	Note1
2	GND	Ground	Note1
3	GND	Ground	Note1
4	DA0-	Pixel data A0	LVDS differential data input Note2
5	DA0+		
6	GND	Ground	Note1
7	DA1-	Pixel data A1	LVDS differential data input Note2
8	DA1+		
9	GND	Ground	Note1
10	DA2-	Pixel data A2	LVDS differential data input Note2
11	DA2+		
12	GND	Ground	Note1
13	CLKA-	Pixel clock A	LVDS differential data input Note2
14	CLKA+		
15	GND	Ground	Note1
16	DA3-	Pixel data A3	LVDS differential data input Note2
17	DA3+		
18	GND	Ground	Note1
19	DA4-	Pixel data A4	LVDS differential data input Note2
20	DA4+		
21	GND	Ground	Note1
22	DB0-	Pixel data B0	LVDS differential data input Note2
23	DB0+		
24	GND	Ground	Note1
25	DB1-	Pixel data B1	LVDS differential data input Note2
26	DB1+		
27	GND	Ground	Note1
28	DB2-	Pixel data B2	LVDS differential data input Note2
29	DB2+		
30	GND	Ground	Note1
31	CLKB-	Pixel clock B	LVDS differential data input Note2
32	CLKB+		
33	GND	Ground	Note1
34	DB3-	Pixel data B3	LVDS differential data input Note2
35	DB3+		
36	GND	Ground	Note1
37	DB4-	Pixel data B4	LVDS differential data input Note2
38	DB4+		
39	GND	Ground	Note1
40	GND	Ground	Note1

To be continued

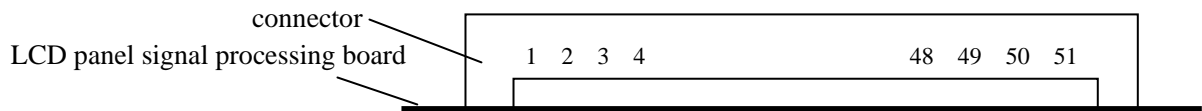
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Continued

Pin No.	Symbol	Signal	Remarks
41	GND	Ground	Note1
42	RESERVED	RESERVED	Keep this pin Open.
43	RESERVED	RESERVED	Keep this pin Open.
44	RESERVED	RESERVED	Keep this pin Open.
45	RESERVED	RESERVED	Keep this pin Open.
46	GND	Ground	Note1
47	EXTPOL	External polarity control input signal	Note3
48	DLPOUT	Data latch pulse output signal	Note4
49	VSPOUT	Gate start pulse output signal	Note4
50	RESERVED	RESERVED	Keep this pin Open.
51	GND	Ground	Note1

2  
2  
2

CN1: Connection inserting side

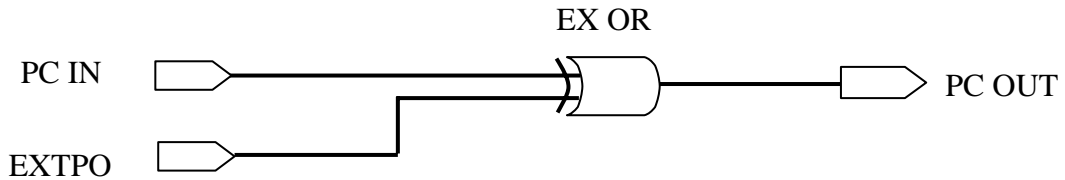


Note1: All GND terminals should be used without any non-connected lines.

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

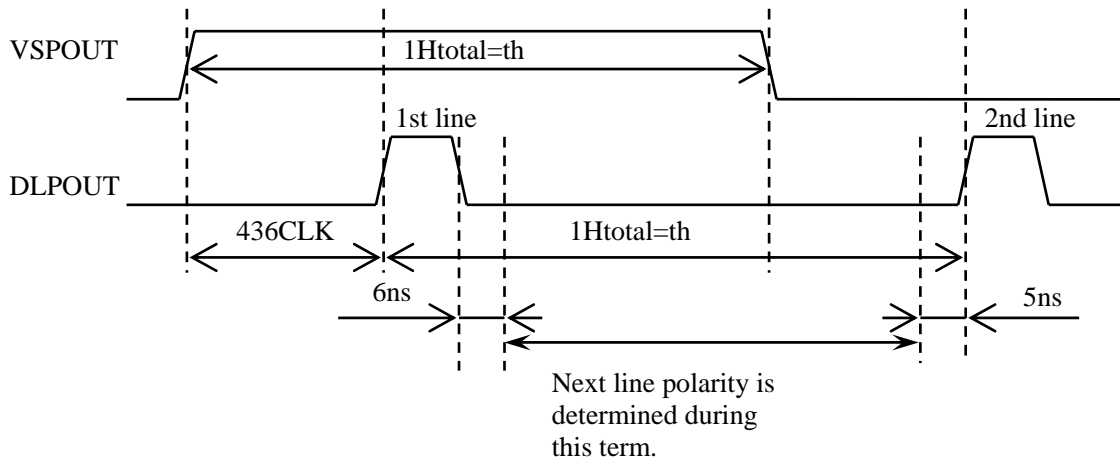
Note3: It is possible to control the polarity inversion to input external signal into No.47pin.

2



Note4: PC input signal to No.47 pin needs to be synchronized with output signals from No.48 and 49.

2



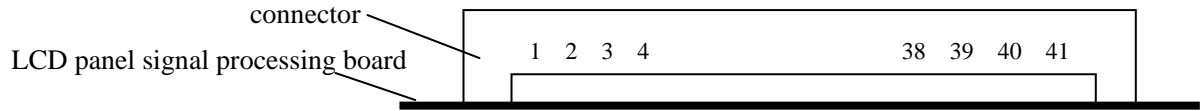
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CN2 socket (LCD module side): FI-RE41S-HS (Japan Aviation Electronics Industry Limited (JAE))  
 Adaptable plug: FI-RE41HL , FI-RE41CL (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	Note1
2	GND	Ground	Note1
3	GND	Ground	Note1
4	DC0-	Pixel data C0	LVDS differential data input Note2
5	DC0+		
6	GND	Ground	Note1
7	DC1-	Pixel data C1	LVDS differential data input Note2
8	DC1+		
9	GND	Ground	Note1
10	DC2-	Pixel data C2	LVDS differential data input Note2
11	DC2+		
12	GND	Ground	Note1
13	CLKC-	Pixel clock C	LVDS differential data input Note2
14	CLKC+		
15	GND	Ground	Note1
16	DC3-	Pixel data C3	LVDS differential data input Note2
17	DC3+		
18	GND	Ground	Note1
19	DC4-	Pixel data C4	LVDS differential data input Note2
20	DC4+		
21	GND	Ground	Note1
22	DD0-	Pixel data D0	LVDS differential data input Note2
23	DD0+		
24	GND	Ground	Note1
25	DD1-	Pixel data D1	LVDS differential data input Note2
26	DD1+		
27	GND	Ground	Note1
28	DD2-	Pixel data D2	LVDS differential data input Note2
29	DD2+		
30	GND	Ground	Note1
31	CLKD-	Pixel clock D	LVDS differential data input Note2
32	CLKD+		
33	GND	Ground	Note1
34	DD3-	Pixel data D3	LVDS differential data input Note2
35	DD3+		
36	GND	Ground	Note1
37	DD4-	Pixel data D4	LVDS differential data input Note2
38	DD4+		
39	GND	Ground	Note1
40	GND	Ground	Note1
41	GND	Ground	Note1

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CN2: Connector inserting side



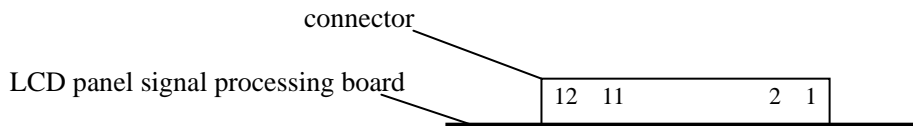
Note1: All GND terminals should be used without any non-connected lines.

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

CN3 socket (LCD module side): IL-Z-12PL1-SMTYE (Japan Aviation Electronics Industry Limited (JAE))  
 Adaptable plug: IL-Z-12S-S125C3 (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	VDD	Power supply	+12V Note1
2	VDD		
3	VDD		
4	VDD		
5	VDD		
6	VDD		
7	GND	Signal ground	Note1
8	GND		
9	GND		
10	GND		
11	GND		
12	GND		

CN3: Connector inserting side



Note1: All VDD and GND terminals should be used without any non-connected lines.

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## 4.5.2 Backlight lamp

CN201 plug(LCD module side):BHR-04VS-1(J.S.T Mfg Co., Ltd)

Adaptable socket: SM04B-BHS-1-TB (J.S.T Mfg Co., Ltd)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage terminal (Hot)	Cable color: Pink
2	N.C.		Keep this pin Open
3	N.C.		Keep this pin Open
4	VBLH	High voltage terminal (Hot)	Cable color: White

CN202 plug(LCD module side):BHR-04VS-1(J.S.T Mfg Co., Ltd)

Adaptable socket: SM04B-BHS-1-TB (J.S.T Mfg Co., Ltd)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage terminal (Hot)	Cable color: Pink
2	N.C.		Keep this pin Open
3	N.C.		Keep this pin Open
4	VBLH	High voltage terminal (Hot)	Cable color: White

CN203 plug(LCD module side):BHR-04VS-1(J.S.T Mfg Co., Ltd)

Adaptable socket: SM04B-BHS-1-TB (J.S.T Mfg Co., Ltd)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage terminal (Hot)	Cable color: Pink
2	N.C.		Keep this pin Open
3	N.C.		Keep this pin Open
4	VBLH	High voltage terminal (Hot)	Cable color: White

CN204 plug(LCD module side):BHR-04VS-1(J.S.T Mfg Co., Ltd)

Adaptable socket: SM04B-BHS-1-TB (J.S.T Mfg Co., Ltd)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage terminal (Hot)	Cable color: Pink
2	N.C.		Keep this pin Open
3	N.C.		Keep this pin Open
4	VBLH	High voltage terminal (Hot)	Cable color: White

CN205 plug(LCD module side):BHR-04VS-1(J.S.T Mfg Co., Ltd)

Adaptable socket: SM04B-BHS-1-TB (J.S.T Mfg Co., Ltd)

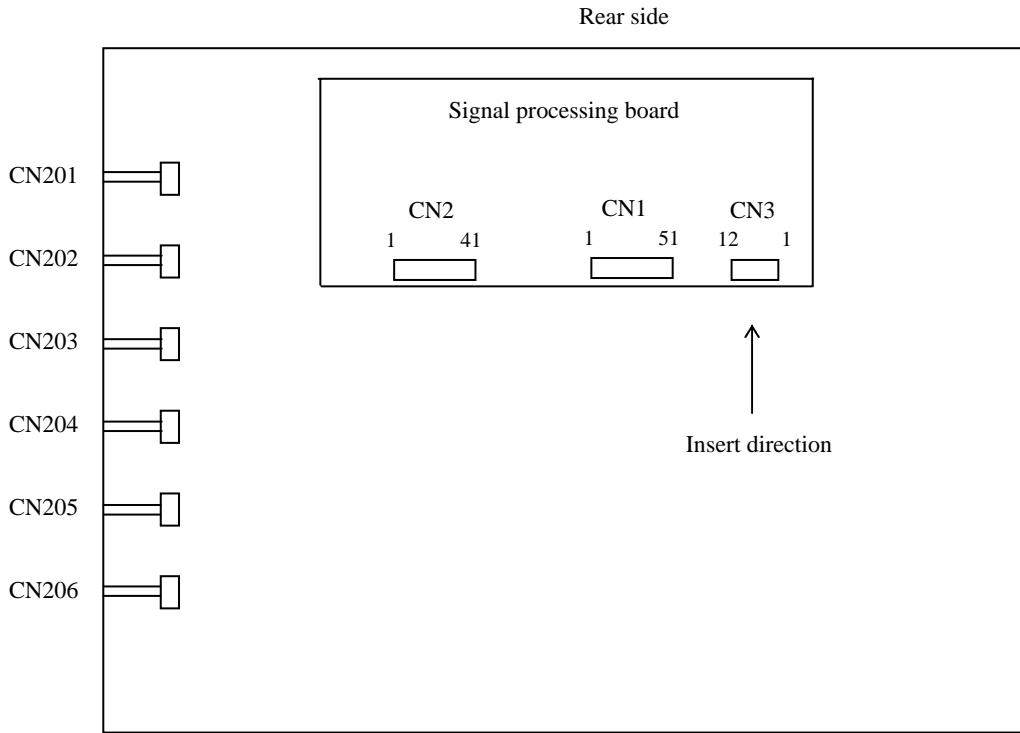
Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage terminal (Hot)	Cable color: Pink
2	N.C.		Keep this pin Open
3	N.C.		Keep this pin Open
4	VBLH	High voltage terminal (Hot)	Cable color: White

CN206 plug(LCD module side):BHR-04VS-1(J.S.T Mfg Co., Ltd)

Adaptable socket: SM04B-BHS-1-TB (J.S.T Mfg Co., Ltd)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage terminal (Hot)	Cable color: Pink
2	N.C.		Keep this pin Open
3	N.C.		Keep this pin Open
4	VBLH	High voltage terminal (Hot)	Cable color: White

### 4.5.3 Positions of socket



2

# PRELIMINARY

## 4.6 METHOD OF CONNECTION FOR LVDS TRANSMITTER

	Bit mapping	Trancemitter Pin Assign		Output Connector	CNI		
		Single type LVDS Tx	Dual type LVDS Tx Thine THC63LVD103		Pin No.	Signal Name	
Pixel data A	RA4	TA0	R14	ATA-	-	-	
	RA5	TA1	R15		4	DA0-	
	RA6	TA2	R16		ATA+	5	DA0+
	RA7	TA3	R17			-	-
	RA8	TA4	R18	ATB-	7	DA1-	
	RA9	TA5	R19		ATB+	8	DA1+
	GA4	TA6	G14			-	-
	GA5	TB0	G15		ATC-	10	DA2-
	GA6	TB1	G16	ATC+		11	DA2+
	GA7	TB2	G17			-	-
	GA8	TB3	G18	ATD-		16	DA3-
	GA9	TB4	G19		ATD+	17	DA3+
	BA4	TB5	B14			-	-
	BA5	TB6	B15		ATE-	19	DA4-
	BA6	TC0	B16	ATE+		20	DA4+
	BA7	TC1	B17			-	-
	BA8	TC2	B18	ATCLK- ATCLK+		13	CLKA-
	BA9	TC3	B19		14	CLKA+	
	Hsync	TC4	Hsync		-	-	
	Vsync	TC5	Vsync		-	-	
	DE	TC6	DE	BTA-	23	DB0+	
	RA2	TD0	R12		BTA+	-	-
	RA3	TD1	R13			-	-
	GA2	TD2	G12		BTB-	25	DB1-
	GA3	TD3	G13	BTB+		26	DB1+
	BA2	TD4	B12			-	-
	BA3	TD5	B13	BTC-		28	DB2-
	N.C.	TD6	-		BTC+	29	DB2+
	RA0	TE0	R10			-	-
	RA1	TE1	R11		BTD-	34	DB3-
	GA0	TE2	G10	BTD+		35	DB3+
	GA1	TE3	G11			-	-
BA0	TE4	B10	BTE-	37		DB4-	
BA1	TE5	B11		BTE+	38	DB4+	
N.C.	TE6	-			-	-	
CLK	CLK	CLK		BTCLK- BTCLK+	31	CLKB-	
			32		CLKB+		
Pixel data B	RB4	TA0	R14	BTA-	-	-	
	RB5	TA1	R15		BTA+	23	DB0+
	RB6	TA2	R16			-	-
	RB7	TA3	R17		BTB-	25	DB1-
	RB8	TA4	R18	BTB+		26	DB1+
	RB9	TA5	R19			-	-
	GB4	TA6	G14	BTC-		28	DB2-
	GB5	TB0	G15		BTC+	29	DB2+
	GB6	TB1	G16			-	-
	GB7	TB2	G17		BTD-	34	DB3-
	GB8	TB3	G18	BTD+		35	DB3+
	GB9	TB4	G19			-	-
	BB4	TB5	B14	BTE-		37	DB4-
	BB5	TB6	B15		BTE+	38	DB4+
	BB6	TC0	B16			-	-
	BB7	TC1	B17		BTCLK- BTCLK+	31	CLKB-
	BB8	TC2	B18	32		CLKB+	
	BB9	TC3	B19	-		-	
	Hsync	TC4	Hsync	-		-	
	Vsync	TC5	Vsync	-	-		
	DE	TC6	DE	BTA-	23	DB0+	
	RB2	TD0	R12		BTA+	-	-
	RB3	TD1	R13			-	-
	GB2	TD2	G12		BTB-	25	DB1-
	GB3	TD3	G13	BTB+		26	DB1+
	BB2	TD4	B12			-	-
	BB3	TD5	B13	BTC-		28	DB2-
	N.C.	TD6	-		BTC+	29	DB2+
	RB0	TE0	R10			-	-
	RB1	TE1	R11		BTD-	34	DB3-
	GB0	TE2	G10	BTD+		35	DB3+
	GB1	TE3	G11			-	-
BB0	TE4	B10	BTE-	37		DB4-	
BB1	TE5	B11		BTE+	38	DB4+	
N.C.	TE6	-			-	-	
CLK	CLK	CLK		BTCLK- BTCLK+	31	CLKB-	
			32		CLKB+		

# PRELIMINARY

	Bit mapping	Trancemitter Pin Assign		Output Connector	CN2				
		Single type LVDS Tx	Dual type LVDS Tx Thine THC63LVD103		Pin No.	Signal Name			
Pixel Data C	RC4	TA0	R14	CTA-	→	-	-		
	RC5	TA1	R15			CTA+	→	5	DC0+
	RC6	TA2	R16					-	-
	RC7	TA3	R17	7	DC1-				
	RC8	TA4	R18	CTB-	→	8	DC1+		
	RC9	TA5	R19			-	-		
	GC4	TA6	G14			CTC-	→	10	DC2-
	GC5	TB0	G15	CTC+	→			11	DC2+
	GC6	TB1	G16					-	-
	GC7	TB2	G17			CTD-	→	16	DC3-
	GC8	TB3	G18	CTD+	→			17	DC3+
	GC9	TB4	G19					-	-
	BC4	TB5	B14			CTE-	→	19	DC4-
	BC5	TB6	B15	CTE+	→			20	DC4+
	BC6	TC0	B16					-	-
	BC7	TC1	B17			CTCLK- CTCLK+	→	13	CLKC-
	BC8	TC2	B18	CTCLK+	→			14	CLKC+
	BC9	TC3	B19					-	-
	Hsync	TC4	Hsync			DTA-	→	23	DD0+
	Vsync	TC5	Vsync	DTA+	→			-	-
	DE	TC6	DE					DTB-	→
	RC2	TD0	R12			DTB+	→		
	RC3	TD1	R13	DTC-	→				
	GC2	TD2	G12					DTC+	→
	GC3	TD3	G13			DTD-	→		
	BC2	TD4	B12	DTD+	→				
	BC3	TD5	B13					-	-
	N.C.	TD6	-			DTE-	→	37	DD4-
	RC0	TE0	R10	DTE+	→			38	DD4+
	RC1	TE1	R11					-	-
	GC0	TE2	G10			DTCLK- DTCLK+	→	31	CLKD-
	GC1	TE3	G11	DTCLK+	→			32	CLKD+
	BC0	TE4	B10					-	-
	BC1	TE5	B11			-	-		
N.C.	TE6	-	-	-					
CLK	CLK	CLK	-	-					
Pixel Data D	RD4	TA0	R14	DTA-	→	-	-		
	RD5	TA1	R15			DTA+	→	23	DD0+
	RD6	TA2	R16					-	-
	RD7	TA3	R17	DTB-	→			25	DD1-
	RD8	TA4	R18			DTB+	→	26	DD1+
	RD9	TA5	R19					-	-
	GD4	TA6	G14	DTC-	→			28	DD2-
	GD5	TB0	G15			DTC+	→	29	DD2+
	GD6	TB1	G16					DTD-	→
	GD7	TB2	G17	DTD+	→				
	GD8	TB3	G18			-	-		
	GD9	TB4	G19			DTE-	→	37	DD4-
	BD4	TB5	B14	DTE+	→			38	DD4+
	BD5	TB6	B15					-	-
	BD6	TC0	B16			DTCLK- DTCLK+	→	31	CLKD-
	BD7	TC1	B17	DTCLK+	→			32	CLKD+
	BD8	TC2	B18					-	-
	BD9	TC3	B19			-	-		
	Hsync	TC4	Hsync	-	-				
	Vsync	TC5	Vsync	-	-				
	DE	TC6	DE	-	-				
	RD2	TD0	R12	-	-				
	RD3	TD1	R13	-	-				
	GD2	TD2	G12	-	-				
	GD3	TD3	G13	-	-				
	BD2	TD4	B12	-	-				
	BD3	TD5	B13	-	-				
	N.C.	TD6	-	-	-				
	RD0	TE0	R10	-	-				
	RD1	TE1	R11	-	-				
	GD0	TE2	G10	-	-				
	GD1	TE3	G11	-	-				
	BD0	TE4	B10	-	-				
	BD1	TE5	B11	-	-				
N.C.	TE6	-	-	-					
CLK	CLK	CLK	-	-					

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

# PRELIMINARY

## 4.7 DISPLAY GRAYSCALE AND INPUT DATA SIGNALS

This product can display in equivalent to 1,073,741,824 colors in 1,024 gray scales. Also the relation between display colors and input data signals is as the following table.

	Display colors	Data signal (0: Low level, 1: High level)																													
		RA9 RA8 RA7 RA6 RA5 RA4 RA3 RA2 RA1 RA0 RB9 RB8 RB7 RB6 RB5 RB4 RB3 RB2 RB1 RB0 RC9 RC8 RC7 RC6 RC5 RC4 RC3 RC2 RC1 RC0 RD9 RD8 RD7 RD6 RD5 RD4 RD3 RD2 RD1 RD0	GA9 GA8 GA7 GA6 GA5 GA4 GA3 GA2 GA1 GA0 GB9 GB8 GB7 GB6 GB5 GB4 GB3 GB2 GB1 GB0 GC9 GC8 GC7 GC6 GC5 GC4 GC3 GC2 GC1 GC0 GD9 GD8 GD7 GD6 GD5 GD4 GD3 GD2 GD1 GD0	BA9 BA8 BA7 BA6 BA5 BA4 BA3 BA2 BA1 BA0 BB9 BB8 BB7 BB6 BB5 BB4 BB3 BB2 BB1 BB0 BC9 BC8 BC7 BC6 BC5 BC4 BC3 BC2 BC1 BC0 BD9 BD8 BD7 BD6 BD5 BD4 BD3 BD2 BD1 BD0																											
Basic Colors	Black	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																											
	Blue	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1																											
	Red	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																											
	Magenta	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1																											
	Green	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0																											
	Cyan	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1																											
	Yellow	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0																											
	White	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1																											
Red gray scale	Black	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																											
	dark	0 0 0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																											
	↑	:	:	:																											
	↓	:	:	:																											
	bright	1 1 1 1 1 1 1 1 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																											
	Red	1 1 1 1 1 1 1 1 0 1	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																											
Green gray scale	Black	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																											
	dark	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0 0 0																											
	↑	:	:	:																											
	↓	:	:	:																											
	bright	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 0 0	0 0 0 0 0 0 0 0 0 0																											
	Green	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 0 1	0 0 0 0 0 0 0 0 0 0																											
Blue gray scale	Black	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0																											
	dark	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 1																											
	↑	:	:	:																											
	↓	:	:	:																											
	bright	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 0 0																											
	Blue	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 0 1																											

## 4.8 INPUT SIGNAL TIMINGS

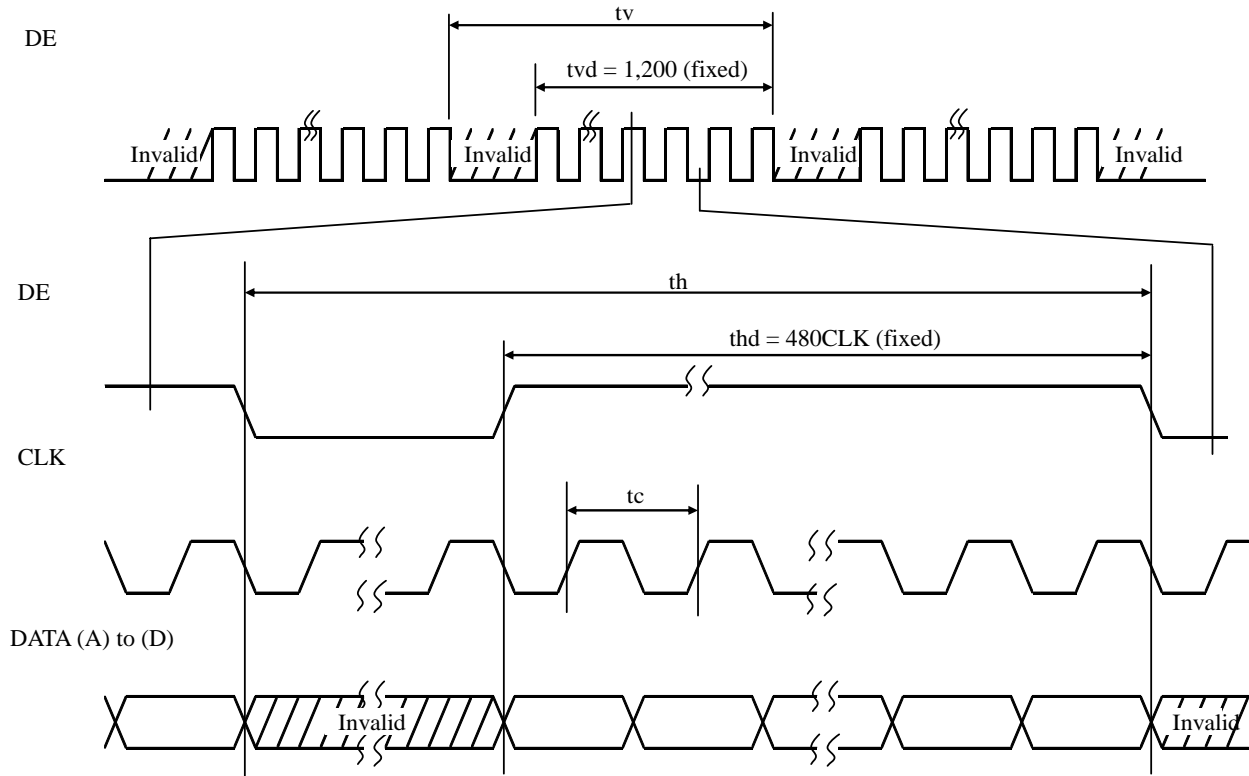
### 4.8.1 Timing characteristics

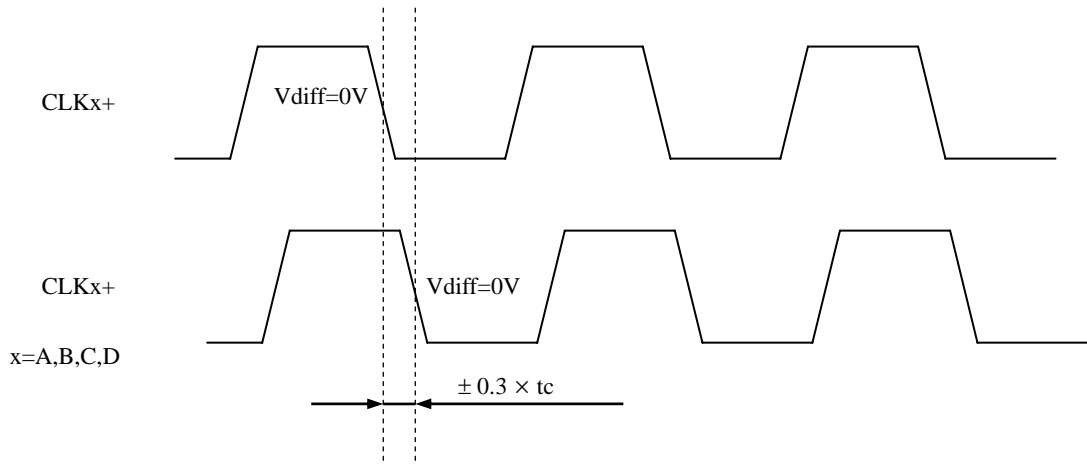
Parameter		Symbol	min.	typ.	max.	Unit	Remarks	
CLK	Frequency		1/tc	(60)	77.0	82.5	MHz	-
			tc	-	12.195	-	ns	
	Rise time, Fall time		-	-			ns	
Duty		-	-			-		
DATA	CLK-DATA	Setup time	-	-			ns	Note1
		Hold time	-	-			ns	
	Rise time, Fall time		-	-			ns	
DE	Horizontal	Cycle	th	6.255 516	6.753 520	(9.351) (720)	$\mu$ s CLK	148.077 kHz (typ.) Note2
		Display period	thd	480			CLK	
	Vertical (One frame)	Cycle	tv	7.530 1,204	8.340 1,235	(10.805) (1,600)	ms H	119.900Hz (typ.)
		Display period	tvd	1,200			H	
	CLK-DE	Setup time	-	-			ns	-
		Hold time	-	-			ns	
Rise time, Fall time		-	-			ns		

Note1: See the data sheet of LVDS transmitter.

Note2: The sum of jitter and skew of horizontal period should be within  $\pm 1$  CLK.

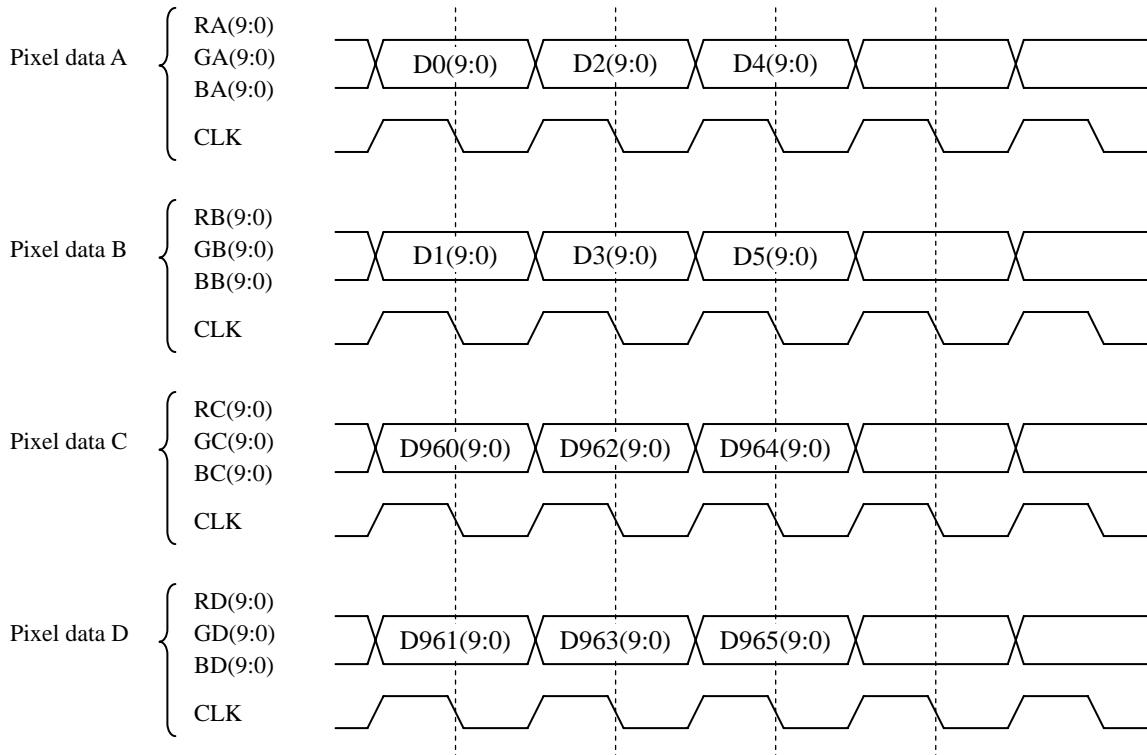
### 4.8.2 Input signal timing chart





2

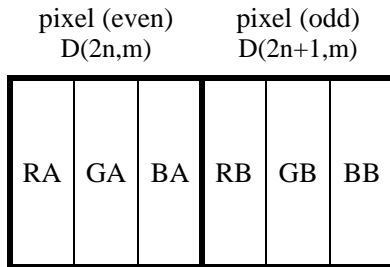
## 4.9 LVDS DATA TRANSMISSION METHOD



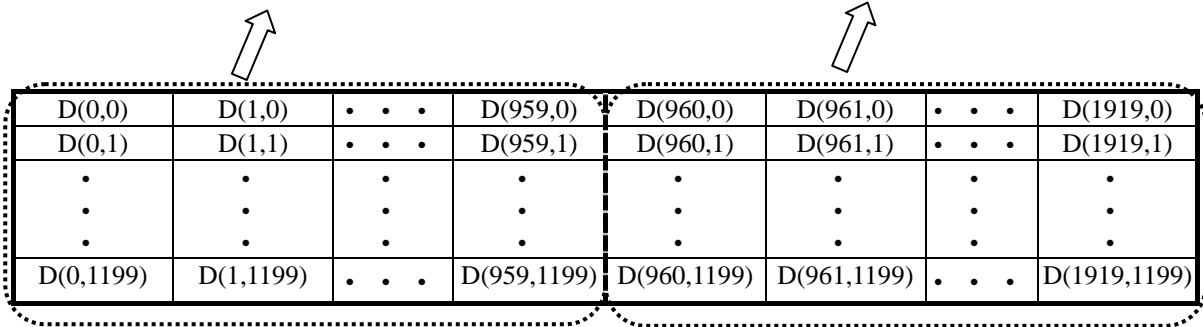
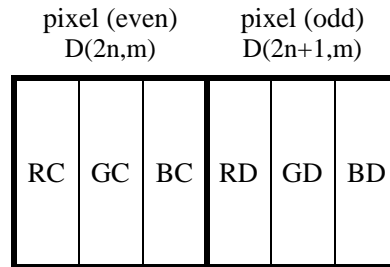
# PRELIMINARY

## 4.10 DISPLAY POSITIONS

Left half of display ( $0 \leq n < 480, 0 \leq m < 1200$ )



Right half of display ( $480 \leq n < 960, 0 \leq m < 200$ )



Note1: n, m: counting number

## 4.11 OPTICS

### 4.11.1 Optical characteristics

(Note1, Note2)

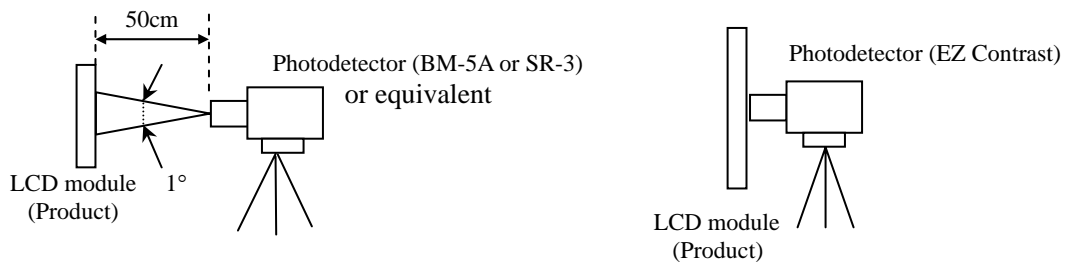
Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks
Luminance		White at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	L	TBD	(500)	-	cd/m <sup>2</sup>	BM-5A or SR-3	-
Contrast ratio		White/Black at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	CR	TBD	(800)	-	-	BM-5A or SR-3	Note3
Luminance uniformity		White $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	LU	TBD	(80)	-	%	BM-5A or SR-3	Note4
Chromaticity	White	x coordinate	W <sub>x</sub>	TBD	(0.313)	TBD	-	SR-3	Note5
		y coordinate	W <sub>y</sub>	TBD	(0.329)	TBD	-		
Response time		Black to White	T <sub>on</sub>	-	(6)	TBD	ms	BM-5A	Note6
		White to Black	T <sub>off</sub>	-	(6)	TBD	ms		Note7
Viewing angle	Right	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	$\theta R$	70	88	-	°	EZ Contrast	Note8
	Left	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	$\theta L$	70	88	-	°		
	Up	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	$\theta U$	70	88	-	°		
	Down	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	$\theta D$	70	88	-	°		

Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.

T<sub>a</sub>=25°C, VDD=12.0V, IBL=(5.0)mA, Luminance control = maximum, Display mode: WUXGA,  
Horizontal cycle= 148.077 kHz, Vertical cycle = 119.900 Hz

Optical characteristics are measured after 20minutes from working the product, in the dark room. Also measurement methods are as follows.



Note3: See "4.11.2 Definition of contrast ratio".

Note4: See "4.11.3 Definition of luminance uniformity".

Note5: These coordinates are found on CIE 1931 chromaticity diagram.

Note6: Product surface temperature: TopF=TBD°C

Note7: See "4.11.4 Definition of response times".

Note8: See "4.11.5 Definition of viewing angles".

### 4.11.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

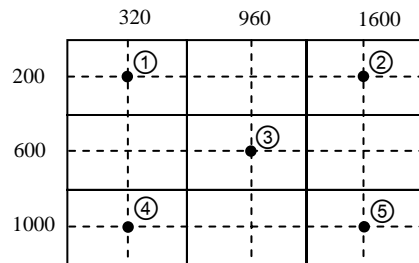
### 4.11.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

$$\text{Luminance uniformity (LU)} = \frac{\text{Minimum luminance from ① to ⑤}}{\text{Maximum luminance from ① to ⑤}}$$

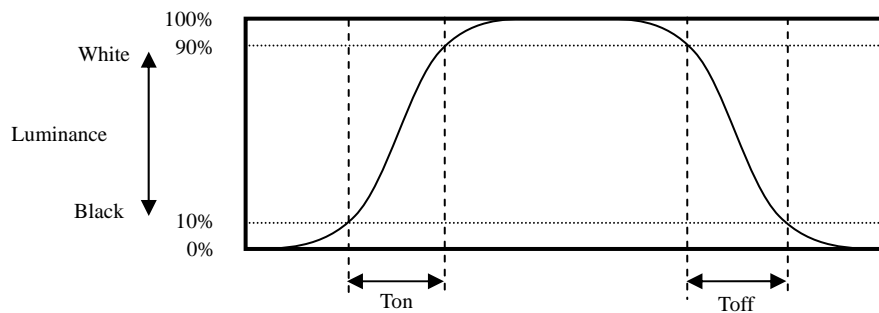
2

The luminance is measured at near the 5 points shown below.

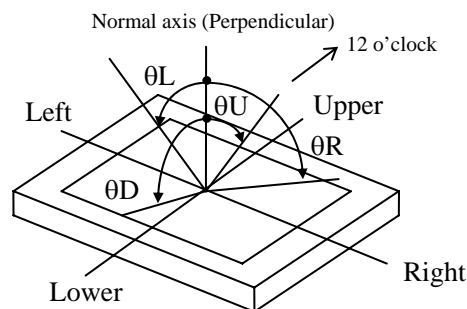


### 4.12.4 Definition of response times

Response time is measured, the luminance changes from " black " to " white ", or " white " to " black " on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



### 4.12.5 Definition of viewing angles



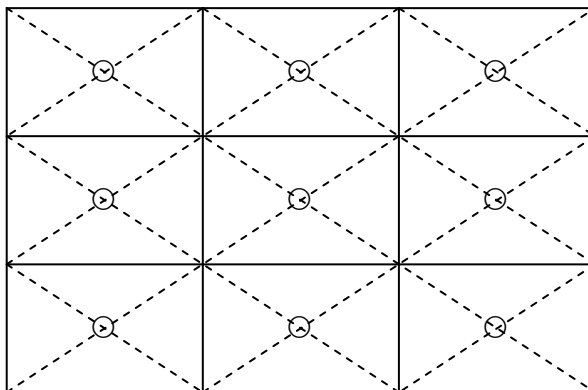
# PRELIMINARY

## 5. RELIABILITY TESTS

Test item	Condition	Judgment Note1
High temperature and humidity (Operation)	① $(60) \pm 2^{\circ}\text{C}$ , RH= 60%, 240hours ② Display data is white.	No display malfunctions
Heat cycle (Operation)	① $0 \pm 3^{\circ}\text{C} \dots 1\text{hour}$ $(50) \pm 3^{\circ}\text{C} \dots 1\text{hour}$ ② 50cycles, 4 hours/cycle ③ Display data is white.	
Thermal shock (Non operation)	① $(-20) \pm 3^{\circ}\text{C} \dots 30\text{minutes}$ $(60) \pm 3^{\circ}\text{C} \dots 30\text{minutes}$ ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
Vibration (Non operation)	① 5 to 100Hz, $11.76\text{m/s}^2$ ② 1 minute/cycle ③ X, Y, Z directions ④ 10 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)	① $294\text{m/s}^2$ , 11ms ② X, Y, Z directions ③ 3 times each directions	
ESD (Operation)	① 150pF, $150\Omega$ , $\pm 10\text{kV}$ ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	No display malfunctions
Dust (Operation)	① Sample dust: No. 15 (by JIS-Z8901)) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.

Note2: See the following figure for discharge points






2


## 6. PRECAUTIONS

### 6.1 MEANING OF CAUTION SIGNS


The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding these contents!**

	This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.
	This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.
	This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

### 6.2 CAUTIONS



**\* Do not touch the working backlight. There is a danger of an electric shock.**



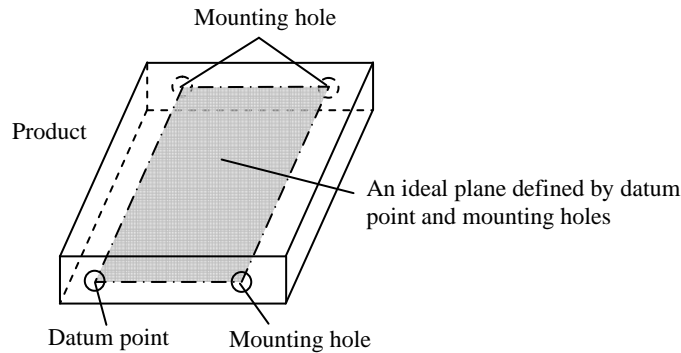
**\* Do not touch the working backlight. There is a danger of burn injury.**  
**\* Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s<sup>2</sup> and to be not greater 11ms, Pressure: To be not greater 19.6N (φ16mm jig))**

### 6.3 ATTENTIONS

#### 6.3.1 Handling of the product

- ① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
- ② Do not hook nor pull cables such as lamp cable, and so on, in order to avoid any damage.
- ③ When the product is put on the table temporarily, display surface must be placed downward.
- ④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
- ⑤ The torque for product mounting screws must never exceed TBDN·m. Higher torque might result in distortion of the bezel.

- ⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura.  
Recommended installing method: An ideal plane that is defined by datum point and mounting holes is to be the same plane within  $\pm 0.2$  mm.



- ⑦ Do not press or rub on the sensitive product surface. When cleaning the product surface, use of the cloth with ethanolic liquid such as screen cleaner for LCD is recommended.
- ⑧ Do not push nor pull the interface connectors while the product is working.
- ⑨ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.
- ⑩ Usually liquid crystals don't leak through the breakage of glasses because of the surface tension of thin layer and the construction of LCD panel. But, if you contact with liquid crystal for the worst, please wash it out with soap.

### 6.3.2 Environment

- ① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
- ② In order to prevent dew condensation occurring by temperature difference, the product packing box should be opened after enough time being left under the environment of an unpacking room. Evaluate the leaving time sufficiently because a situation of dew condensation occurring is changed by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with packing state)
- ③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
- ④ This product is not designed as radiation hardened.

### 6.3.3 Characteristics

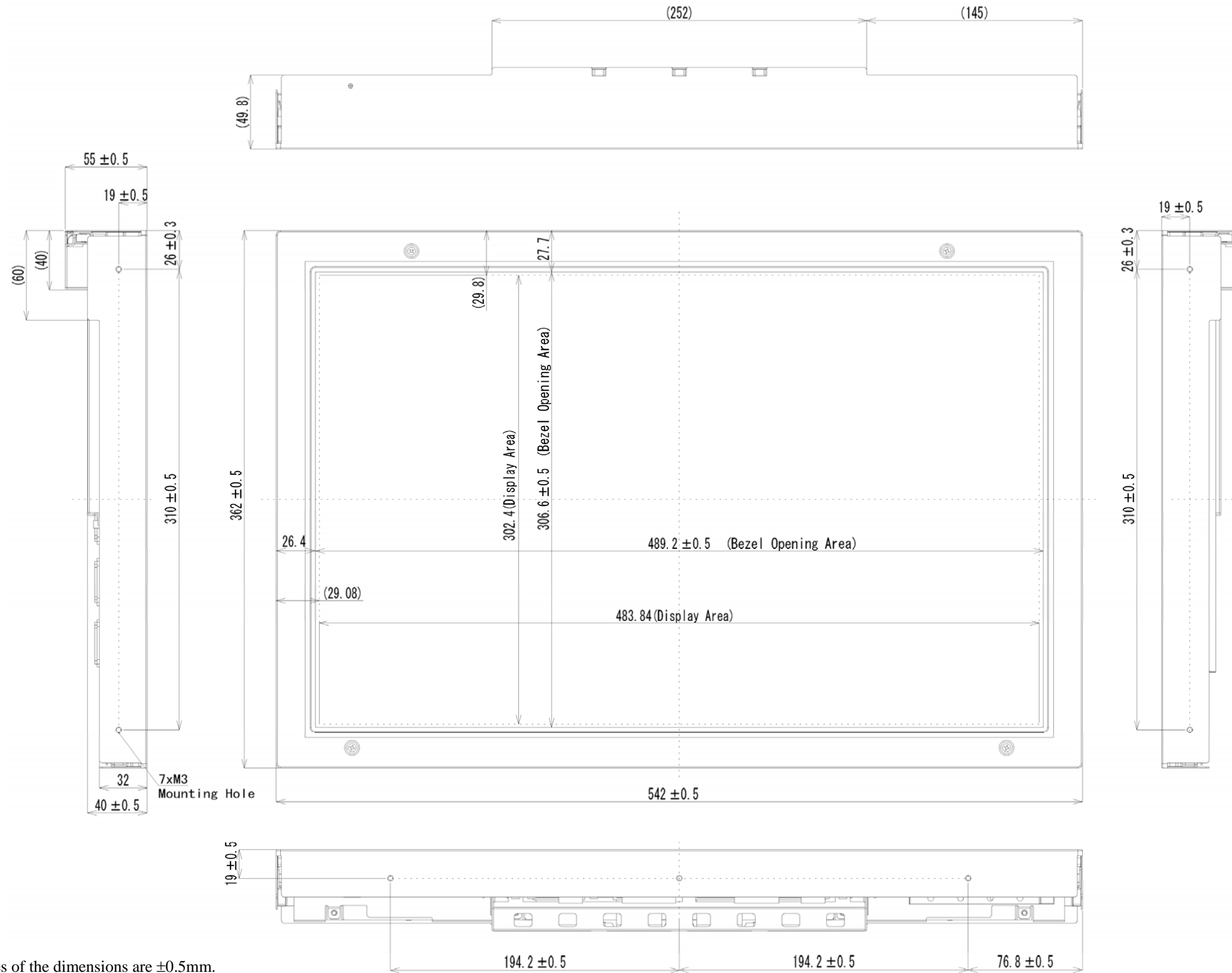
**The following items are neither defects nor failures.**

- ① Response time, luminance and color may be changed by ambient temperature.
- ② Display mura, flicker, vertical seam or small spot may be observed depending on display patterns.
- ③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
- ④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
- ⑤ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
- ⑥ Optical characteristics may be changed depending on input signal timings.
- ⑦ The interference noise between input signal frequency for this product's signal processing board and luminance control frequency of the inverter may appear on a display. Set up luminance control frequency of the inverter so that the interference noise does not appear.

### 6.3.4 Other

- ① All GND and VDD terminals should be used without any non-connected lines.
- ② Do not disassemble a product or adjust variable resistors.
- ③ Pack the product with original shipping package, in order to avoid any damages during transportation, when returning the product to NEC for repair and so on.
- ④ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.

7. OUTLINE DRAWINGS  
7.1 FRONT VIEW

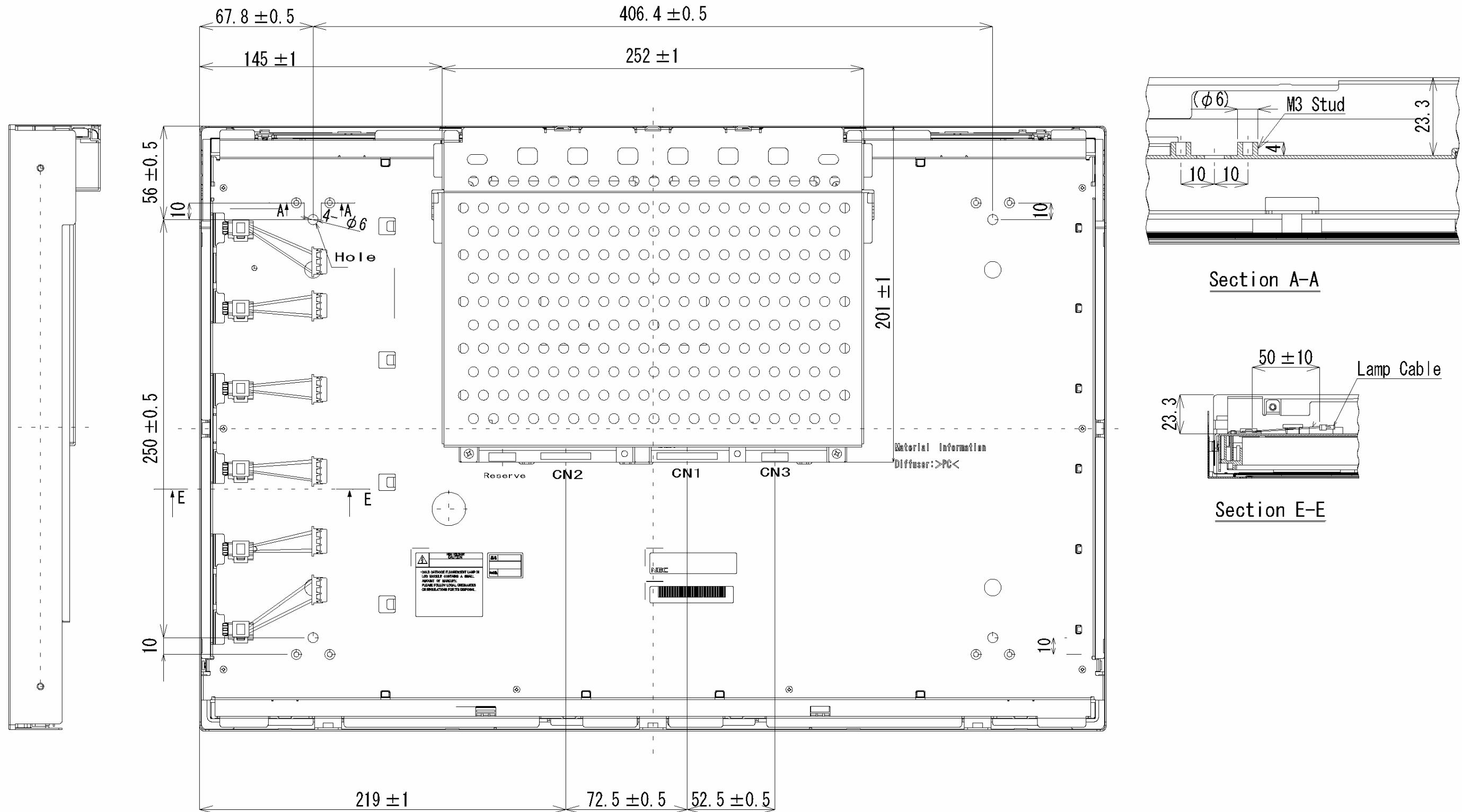


- Note1: Not shown tolerances of the dimensions are ±0.5mm.
- Note2: The torque for product mounting screws must never exceed TBD N·m.
- Note3: The length of product mounting screws from surface of plate must be ≤ TBD mm.
- Note4: The values in parentheses are for reference.

Unit: mm

7.2 REAR VIEW

2




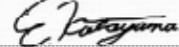
Note1: Not shown tolerances of the dimensions are  $\pm 0.5$ mm.

Unit: mm

# PRELIMINARY

## REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Document number	Prepared date	Revision contents and signature
1st edition	DOD-PP-0407	Nov. 19, 2007	<p><b>Revision contents</b></p> <p>New issue</p> <p><b>Writer</b>  <i>Approved by</i> _____ <i>Checked by</i> _____ <i>Prepared by</i> _____                      T. OGAWA _____ E. KATAYAMA _____</p>
2nd edition	DOD-PP-0543	May 28, 2008	<p><b>Revision contents</b></p> <p>P4 Structure and principle</p> <ul style="list-style-type: none"> <li>NL192120AC25-03 → NL192120BC25-03(correction)</li> </ul> <p>P4 Features</p> <ul style="list-style-type: none"> <li>Super-Advanced Super Fine TFT (SA-SFT) → Ultra-Advanced Super Fine TFT (UA-SFT) (correction)</li> </ul> <p>P5 General specifications</p> <ul style="list-style-type: none"> <li>Designed viewing direction: <math>\gamma=2.2 \rightarrow \gamma \approx 2.2</math></li> <li>Luminance: At the maximum luminance control, (350) cd/m<sup>2</sup> (typ.) → At IBL = (5.0)mArms, (500) cd/m<sup>2</sup> (typ.)</li> <li>Power supply voltage: Inverter: 12.0V (elimination)</li> </ul> <p>P5 General specifications, P7 Mechanical specifications</p> <ul style="list-style-type: none"> <li>Weight: TBD g (typ.) → (3,300) g (typ.)</li> </ul> <p>P5 General specifications, P25 Optical characteristics</p> <ul style="list-style-type: none"> <li>Viewing angle (θR, θL, θU, θD) (°): 85 (typ.) → 88 (typ.)</li> </ul> <p>P6 Block diagram</p> <ul style="list-style-type: none"> <li>VBLC (elimination)</li> <li>Note1 (change)</li> </ul> <p>P8 Electrical characteristics - LCD panel signal processing board</p> <ul style="list-style-type: none"> <li>Power supply voltage: (10.8) V (min.), (13.2) V (max.) → 10.8 V (min.), 13.2 V (max.)</li> <li>Power supply current: TBD mA (max.) → (1,800) mA (max.)</li> </ul> <p>P9 Backlight lamp</p> <ul style="list-style-type: none"> <li>Lamp current: (4.0)(typ.), at IBL= TBD mArms: L= TBD cd/m<sup>2</sup> → (5.0), at IBL= (5.0) mArms: L= (500) cd/m<sup>2</sup></li> </ul> <p>P14 LCD panel signal processing board – CN1 socket</p> <ul style="list-style-type: none"> <li>Pin No.47, 48, 49 (change)</li> <li>Note3, Note4 (addition)</li> </ul> <p>P18 Position of socket (specified)</p> <p>P23 Input signal timing chart (Chart is added.)</p> <p>P24 Pixel arrangement (elimination)</p> <p>P25 Optics - Optical characteristics</p> <ul style="list-style-type: none"> <li>Luminance: (350) cd/m<sup>2</sup> (typ.) → (500) cd/m<sup>2</sup> (typ.)</li> <li>Note2 (change)</li> </ul> <p>P26 Definition of luminance uniformity</p> <ul style="list-style-type: none"> <li>Maximum ↔ Minimum (correction)</li> </ul> <p>P26 Reliability tests</p> <ul style="list-style-type: none"> <li>Image retention (elimination)</li> </ul> <p>P30 Attentions - Other</p> <ul style="list-style-type: none"> <li>Ⓢ (elimination)</li> </ul> <p>P31 Outline Drawings - Front view (revised)</p> <ul style="list-style-type: none"> <li>Note2, Note3, Note4 (addition)</li> </ul> <p>P32 Outline Drawings - Rear view (revised)</p> <p><b>Signature of writer</b></p> <p><i>Approved by</i> _____ <i>Checked by</i> _____ <i>Prepared by</i> _____   _____  _____                      T. OGAWA _____ E. KATAYAMA _____</p>