

TFT LCD Approval Specification

MODEL NO.: V370H1 - L02

Customer: _____

Approval by: _____

Note:

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 2.0	Aug.09,'05	All	All	Approval Specification was first issued.
Ver 2.1	Nov.30,'05	All	All	The remark at the bottom of every page has to be deleted.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V370H1-L02 is a 37" TFT Liquid Crystal Display module with 20-CCFL Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 HDTV format and can display true 16.7M colors (8-bit/color). The inverter module for backlight is build-in.

1.2 FEATURES

- High brightness (600 nits)
- High contrast ratio (1000:1)
- Fast response time
- High color saturation NTSC 75%
- HDTV (1920 x 1080 pixels) resolution, true HDTV format .
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 50/60Hz frame rate
- Ultra wide viewing angle : 176(H)/176(V) (CR>20) Super MVA technology
- 180 degree rotation display option

1.3 APPLICATION

- TFT LCD TVs

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	820.8(H) x 461.7 (V) (37.07" diagonal)	mm	(1)
Bezel Opening Area	828.8 (H) x 470.9 (V)	mm	
Driver Element	a-si TFT active matrix	-	
Pixel Number	1920 x R.G.B. x 1080	pixel	
Pixel Pitch (Sub Pixel)	0.1425 (H) x 0.4275 (V)	mm	
Pixel Arrangement	RGB vertical stripe	-	
Display Colors	16.7M	color	
Display Operation Mode	Transmissive mode / Normally black	-	
Surface Treatment	Hardness (3H), Haze : 40% Anti-reflective coating < less 2% reflection	-	

1.5 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note	
Module Size	Horizontal(H)	884.1	884.8	885.5	mm	
	Vertical(V)	525.0	525.9	526.8	mm	
	Depth(D)	43.34	44.34	45.34	mm	To PCB cover
	Depth(D)	50.74	52.24	53.74	mm	To inverter cover
Weight	8950	9150	9350	g		

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)
Shock (Non-Operating)	S _{NOF}	-	50	G	(3), (5)
Vibration (Non-Operating)	V _{NOF}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

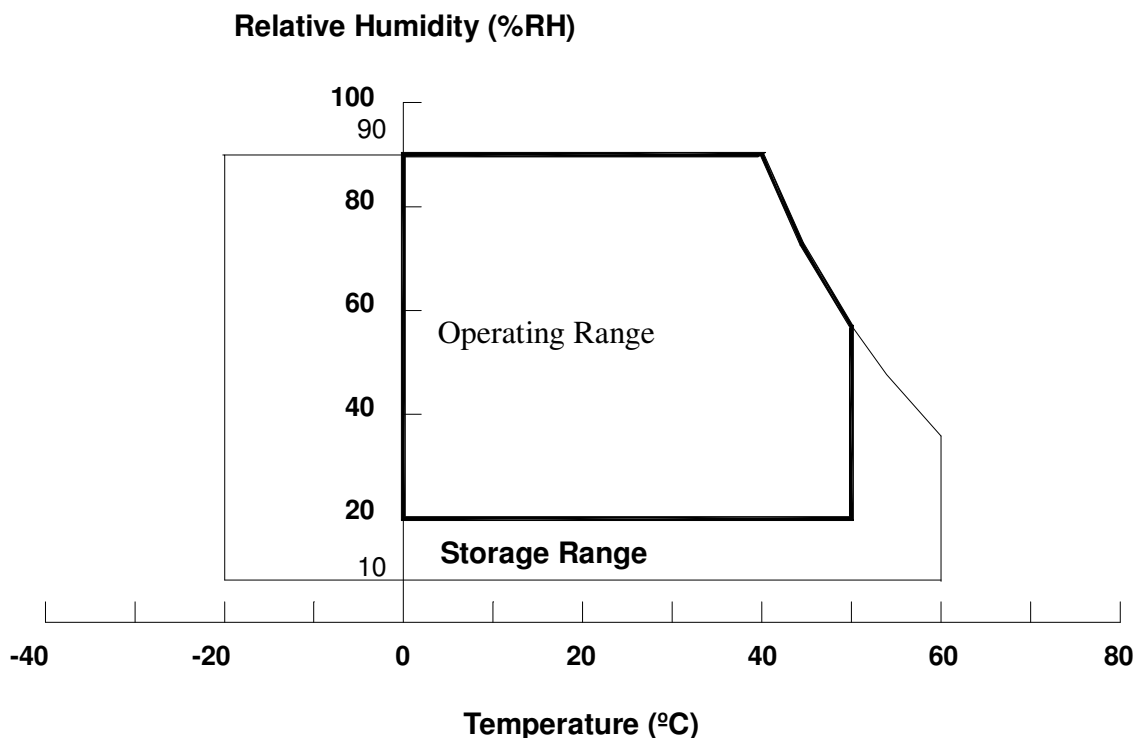
- (a) 90 %RH Max. ($T_a \leq 40$ °C).
- (b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40$ °C).
- (c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 60 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 60 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for $\pm X$, $\pm Y$, $\pm Z$.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V _{CC}	-0.3	20	V	(1)
Input Signal Voltage	V _{IN}	-0.3	(3.6)	V	

2.2.2 BACKLIGHT INVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V _W	—	3000	V _{RMS}	
Power Supply Voltage	V _{BL}	0	140	V	(1)
Auxiliary Power Supply Voltage	V _{AUX}	0	23	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals includes On/Off Control, Internal PWM Control, External PWM Control and Internal/External PWM Selection.

3. ELECTRICAL CHARACTERISTICS

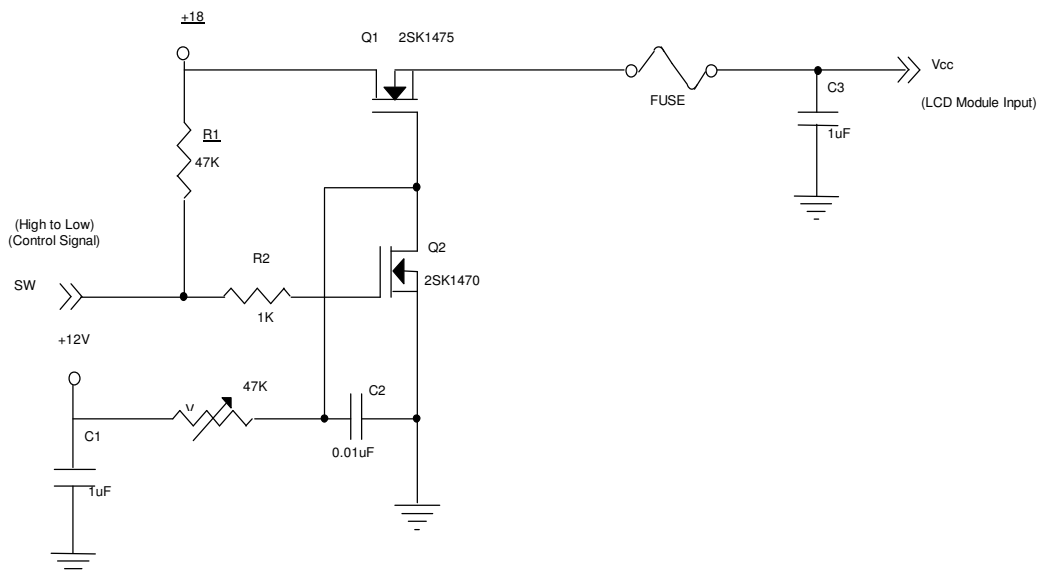
3.1 TFT LCD MODULE

Ta = 25 ± 2 °C

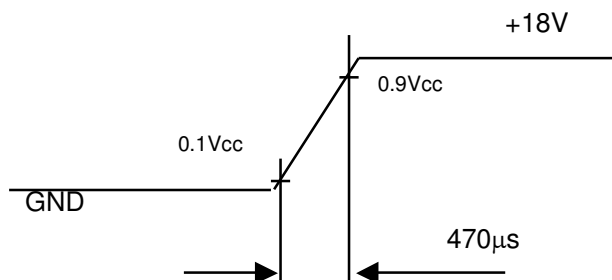
Parameter	Symbol	Value			Unit	Note	
		Min.	Typ.	Max.			
Power Supply Voltage	V _{CC}	16.2	18	19.8	V	(1)	
Power Supply Ripple Voltage	V _{RP}	-	-	200	mV		
Rush Current	I _{RUSH}	-	-	3.5	A	(2)	
Power Supply Current	White	I _{CC}	-	0.80	-	A	(3)
	Black		-	0.45	-	A	
	Vertical Stripe		-	0.65	-	A	
LVDS Interface	Differential Input High Threshold Voltage	V _{LVTH}	-	-	+100	mV	
	Differential Input Low Threshold Voltage	V _{LVTL}	-100	-	-	mV	
	Common Input Voltage	V _{LVC}	1.125	1.25	1.375	V	
	Terminating Resistor	R _T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V _{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	-	0.7	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470μs



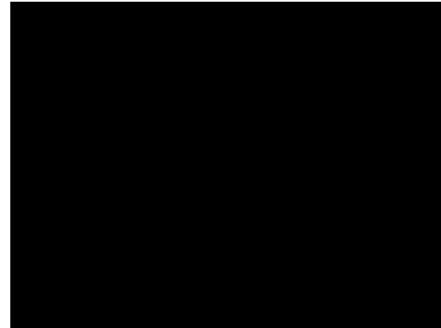
Note (3) The specified power supply current is under the conditions at $V_{CC} = 18\text{ V}$, $T_a = 25 \pm 2\text{ }^\circ\text{C}$, $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



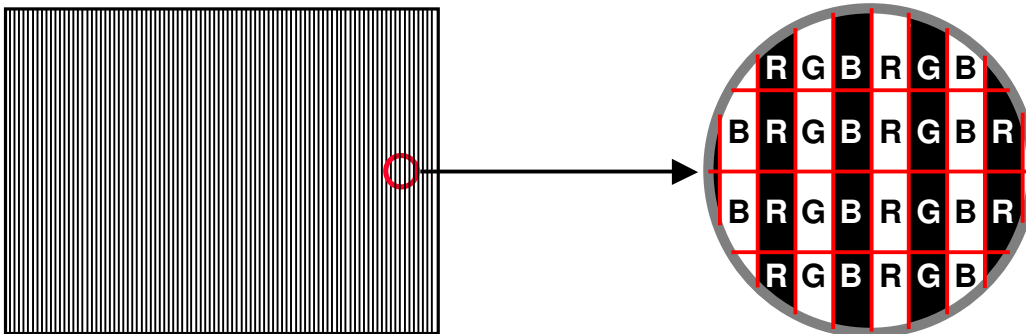
Active Area

b. Black Pattern



Active Area

c. Vertical Stripe Pattern



Active Area

3.2 BACKLIGHT UNIT

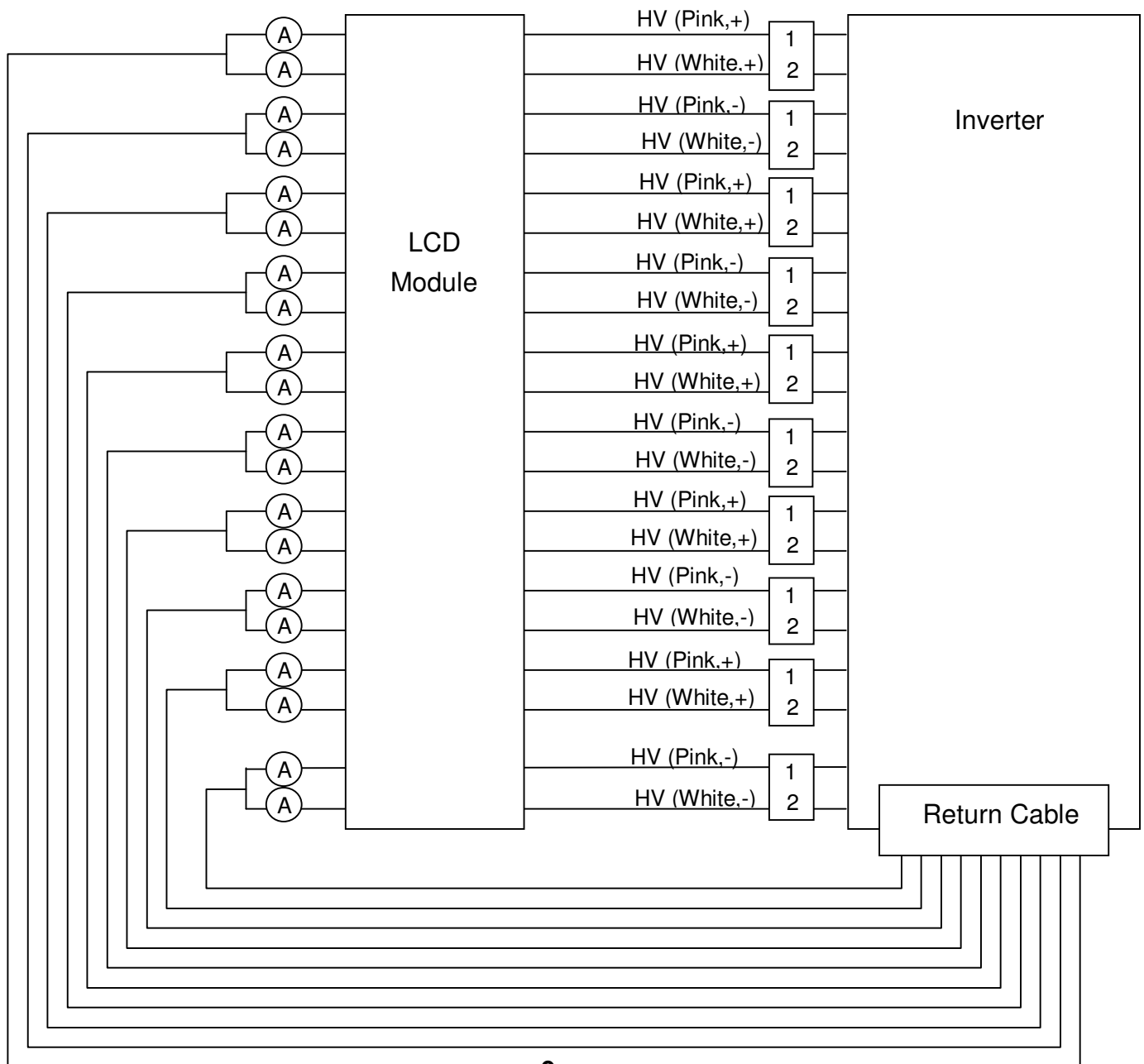
3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS ($T_a = 25 \pm 2\text{ }^\circ\text{C}$)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Voltage	V_W	-	1320	-	V_{RMS}	$I_L = 4.8\text{ mA}$
Lamp Current	I_L	4.3	4.8	5.3	mA_{RMS}	(1)
Lamp Starting Voltage	V_S	-	-	2780	V_{RMS}	(2), $T_a = 0\text{ }^\circ\text{C}$
		-	-	2440	V_{RMS}	(2), $T_a = 25\text{ }^\circ\text{C}$
Operating Frequency	F_L	40	-	70	KHz	(3)
Lamp Life Time	L_{BL}	50,000	60,000	-	Hrs	(4)

3.2.2 INVERTER CHARACTERISTICS ($T_a = 25 \pm 2 \text{ }^\circ\text{C}$)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power consumption	P_{BL}	-	156	-	W	(5), $I_L = 4.8\text{mA}$
Power Supply Voltage	V_{BL}	114	120	126	V_{DC}	
Power Supply Current	I_{BL}	-	1.3	-	A	Non Dimming
Auxiliary Power Supply Voltage	V_{AUX}	17	18	19	V_{DC}	
Auxiliary Power Supply Current	I_{AUX}	-	-	200	mA	
Input Ripple Noise	-	-	-	2.5	V_{P-P}	$V_{BL} = 114\text{V}$
Backlight Turn on Voltage	V_{BS}	2780	-	-	V_{RMS}	$T_a = 0 \text{ }^\circ\text{C}$
		2440	-	-	V_{RMS}	$T_a = 25 \text{ }^\circ\text{C}$
Oscillating Frequency	F_W	51	54	57	kHz	
Dimming frequency	F_B	150	160	170	Hz	
Minimum Duty Ratio	D_{MIN}	-	20	-	%	

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:



Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at $T_a = 25 \pm 2$ °C and $I_L = 4.3 \sim 5.3$ mArms.

Note (5) The power supply capacity should be higher than the total inverter power consumption P_{BL} . Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

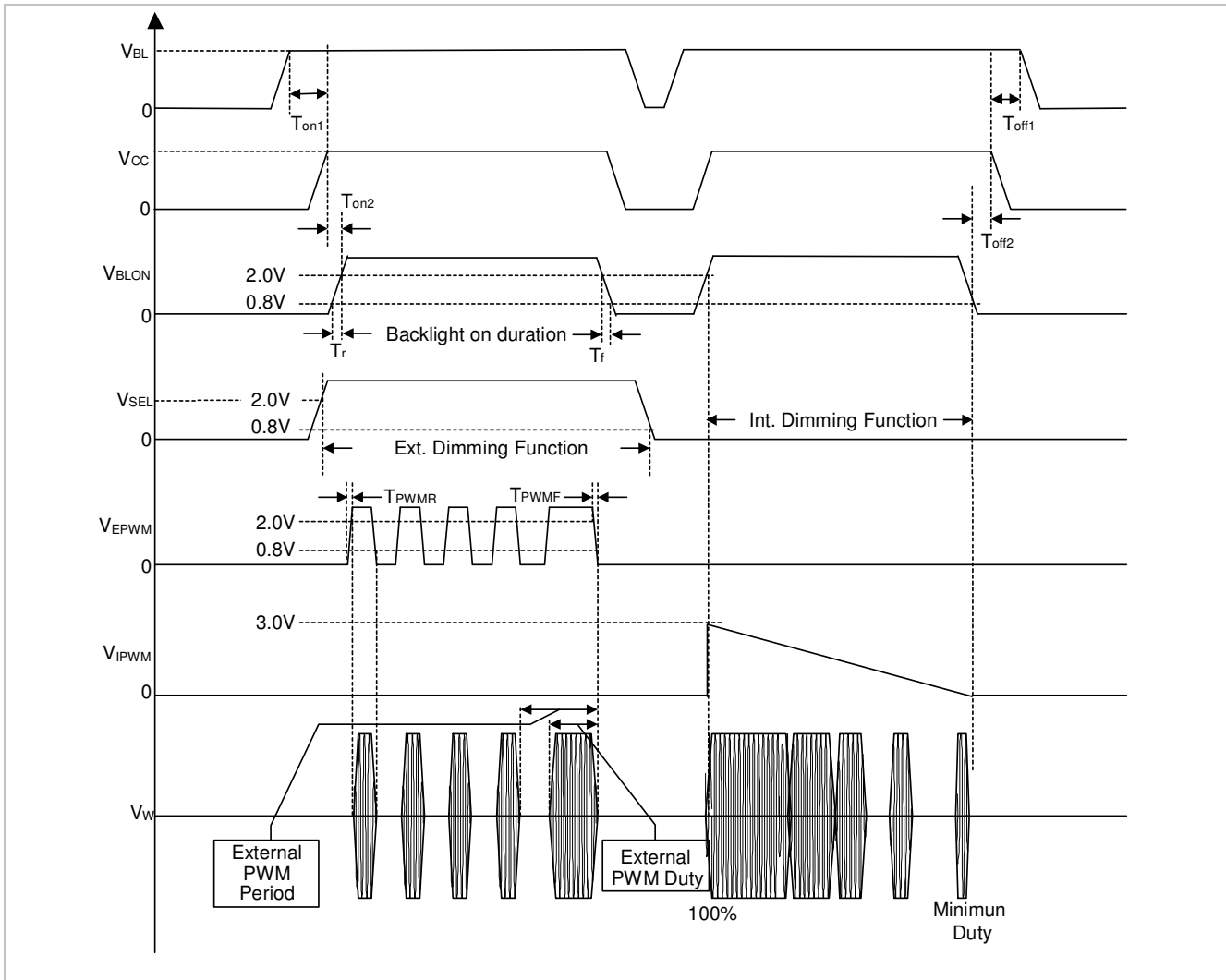
3.2.3 INVERTER INTERFACE CHARACTERISTICS

Parameter	Symbol	Test Condition	Value			Unit	Note	
			Min.	Typ.	Max.			
Inverter Good Signal	HI	V_{IG}	$V_{IG} = \text{High}$	2.0	—	5.0	V	normal Output
	LO		$V_{IG} = \text{Low}$	0	—	0.8	V	abnormal Output
On/Off Control Voltage	ON	V_{BLON}	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal/External PWM Select Voltage	HI	V_{SEL}	—	2.0	—	5.0	V	
	LO		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	V_{IPWM}	$V_{SEL} = L$	—	—	3.0	V	maximum duty ratio
	MIN			—	0	—	V	minimum duty ratio
External PWM Control Voltage	HI	V_{EPWM}	$V_{SEL} = H$	2.0	—	5.0	V	duty on
	LO			0	—	0.8	V	duty off
Control Signal Rising Time	T_r	—	—	—	100	ms		
Control Signal Falling Time	T_f	—	—	—	100	ms		
PWM Signal Rising Time	T_{PWR}	—	—	—	50	us		
PWM Signal Falling Time	T_{PWF}	—	—	—	50	us		
Input impedance	R_{IN}	—	1	—	—	MΩ		
BLON Delay Time1	T_{on1}	—	1	—	—	ms		
BLON Off Time1	T_{off1}	—	1	—	—	ms		
BLON Delay Time2	T_{on2}	—	1	—	—	ms		
BLON Off Time2	T_{off2}	—	1	—	—	ms		

Note(1) The SEL signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM selection (SEL) during backlight turn on period.

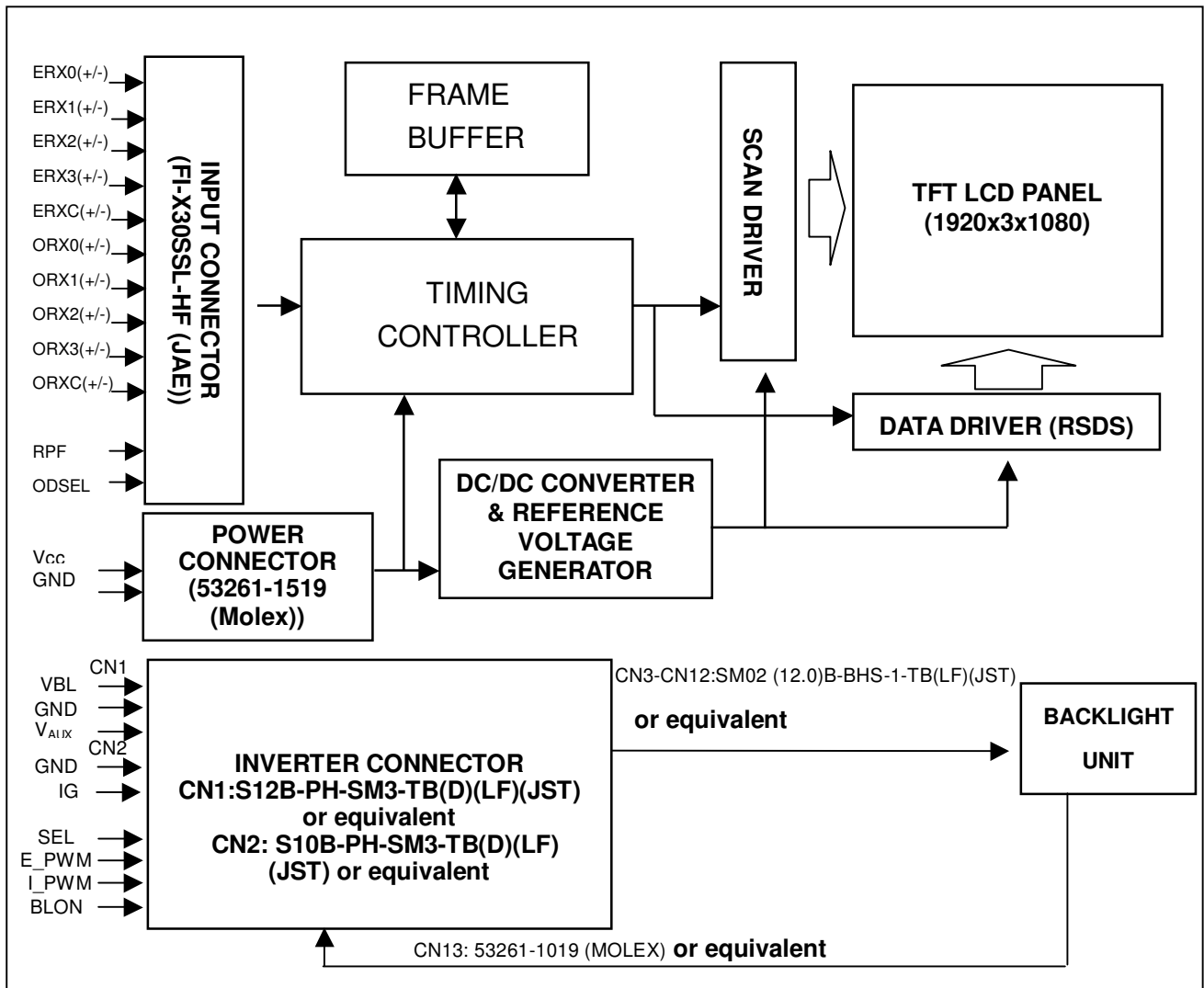
Note(2) The power sequence and control signal timing are shown in the following figure.

Note(3) The power sequence and control signal timing must follow the figure below. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.



4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



5. INTERFACE PIN CONNECTION

5.1 TFT LCD MODULE

CNF1 Connector Pin Assignment

Pin No.	Symbol	Description	Note
1	NC	No Connection	(4)
2	RPF	Display Rotation	(3)
3	NC	No Connection	(4)
4	NC	No Connection	
5	NC	No Connection	
6	ODSEL	Overdrive Lookup Table Selection	(5)
7	NC	No Connection	(4)
8	GND	Ground	
9	ERX0-	Negative transmission data of Even pixel 0	
10	ERX0+	Positive transmission data of Even pixel 0	
11	ERX1-	Negative transmission data of Even pixel 1	
12	ERX1+	Positive transmission data of Even pixel 1	
13	ERX2-	Negative transmission data of Even pixel 2	
14	ERX2+	Positive transmission data of Even pixel 2	
15	ECLK-	Negative of Even clock	
16	ECLK+	Positive of Even clock	
17	ERX3-	Negative transmission data of Even pixel 3	
18	ERX3+	Positive transmission data of Even pixel 3	
19	GND	Ground	
20	ORX0-	Negative transmission data of Odd pixel 0	
21	ORX0+	Positive transmission data of Odd pixel 0	
22	ORX1-	Negative transmission data of Odd pixel 1	
23	ORX1+	Positive transmission data of Odd pixel 1	
24	ORX2-	Negative transmission data of Odd pixel 2	
25	ORX2+	Positive transmission data of Odd pixel 2	
26	OCLK-	Negative of Odd clock	
27	OCLK+	Positive of Odd clock	
28	ORX3-	Negative transmission data of Odd pixel 3	
29	ORX3+	Positive transmission data of Odd pixel 3	
30	GND	Ground	

CNF2 Connector Pin Assignment

Pin No.	Symbol	Description	Note
1	VCC	+18.0V power supply	
2	VCC	+18.0V power supply	
3	VCC	+18.0V power supply	
4	VCC	+18.0V power supply	
5	VCC	+18.0V power supply	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	GND	Ground	
11	NC	No Connection	(4)
12	NC	No Connection	
13	NC	No Connection	
14	NC	No Connection	

15	NC	No Connection	
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Note (1) CNF1 Connector part no.: FI-X30SSL-HF (JAE) or equivalent.

Note (2) CNF2 Connector part no.: 53261-1519 (Molex) or equivalent.

Note (3) Low : normal display (default), High : display with 180 degree rotation

Note (4) Reserved for internal use. Left it open.

Note (5) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance to the frame rate to optimize image quality.

ODSEL	Note
L	Lookup table was optimized for 60 Hz frame rate.
H	Lookup table was optimized for 50 Hz frame rate.

5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN3-CN12: BHR-04VS-1 (JST).

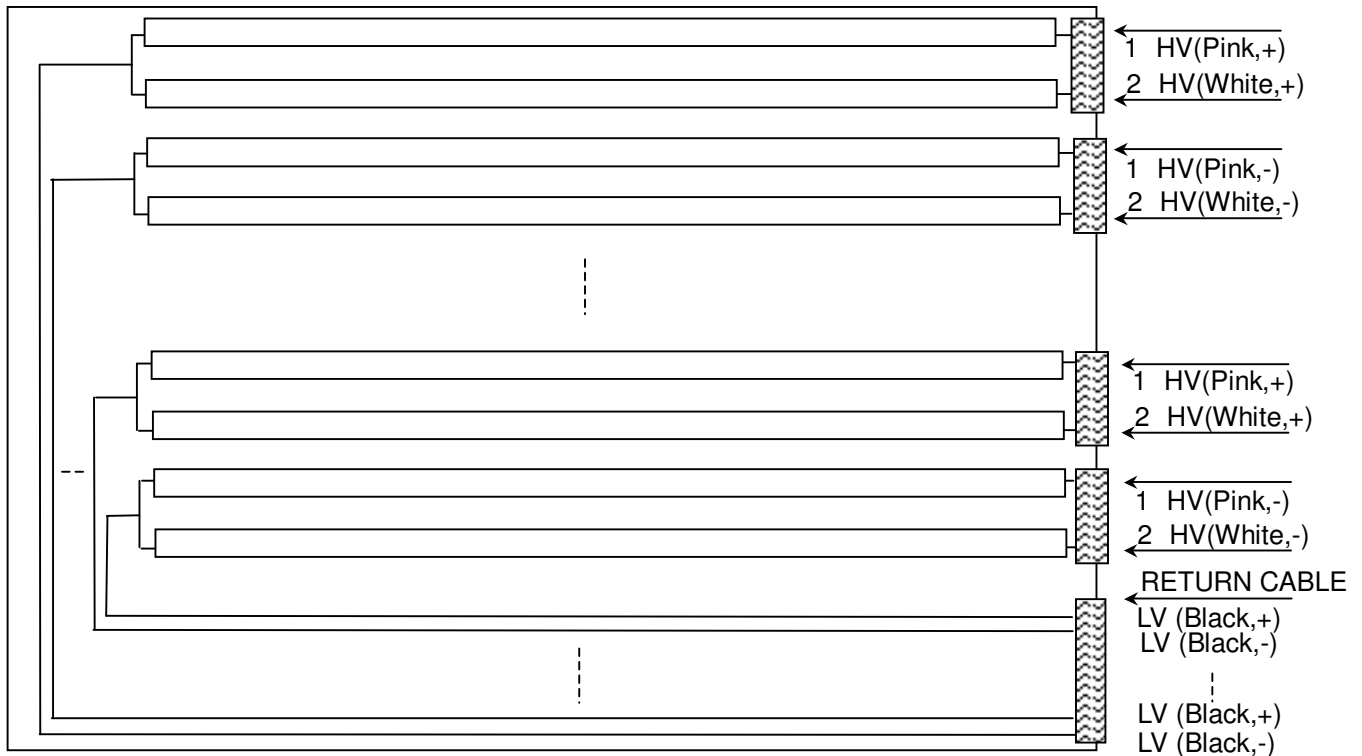
Pin No.	Symbol	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model BHR-04VS-1, manufactured by JST.
 The mating header on inverter part number is SM02(12.0)B-BHS-1-TB(LF).

CN13: 51021-1000 (MOLEX) or equivalent

Pin No.	Symbol	Description	Wire Color
1	LV	Low Voltage	Black
2	LV	Low Voltage	Black
3	LV	Low Voltage	Black
4	LV	Low Voltage	Black
5	LV	Low Voltage	Black
6	LV	Low Voltage	Black
7	LV	Low Voltage	Black
8	LV	Low Voltage	Black
9	LV	Low Voltage	Black
10	LV	Low Voltage	Black

Note(2) The backlight interface housing and return cable for low voltage side is a model 51021-1000, manufactured by MOLEX or equivalent. The mating header on inverter part number is 53261-1019 (MOLEX) or equivalent.



5.3 INVERTER UNIT

CN1(Header): S12B-PH-SM3-TB (D)(LF)(JST) or equivalent.

Pin No.	Symbol	Description
1	VBL	+120V _{DC} Power input
2		
3		
4	NC	NC
5		
6		
7	GND	GND
8		
9		
10		
11	V _{AUX}	18V _{DC}
12		

CN2(Header): S10B-PH-SM3-TB (D)(LF)(JST) or equivalent

Pin No.	Symbol	Description
1	GND	GND
2		
3		
4	NC	NC
5	IG	Inverter Good Signal
6	NC	NC
7	SEL	Internal/external PWM selection High : external dimming Low : internal dimming
8	E_PWM	External PWM control signal E_PWM should be connected to ground when internal PWM was selected (SEL = low).
9	I_PWM	Internal PWM control signal I_PWM should be connected to ground when external PWM was selected (SEL = high).
10	BLON	Backlight on/off control

CN3-CN12(Header): SM02(12.0)B-BHS-1-TB (LF)(JST) or equivalent

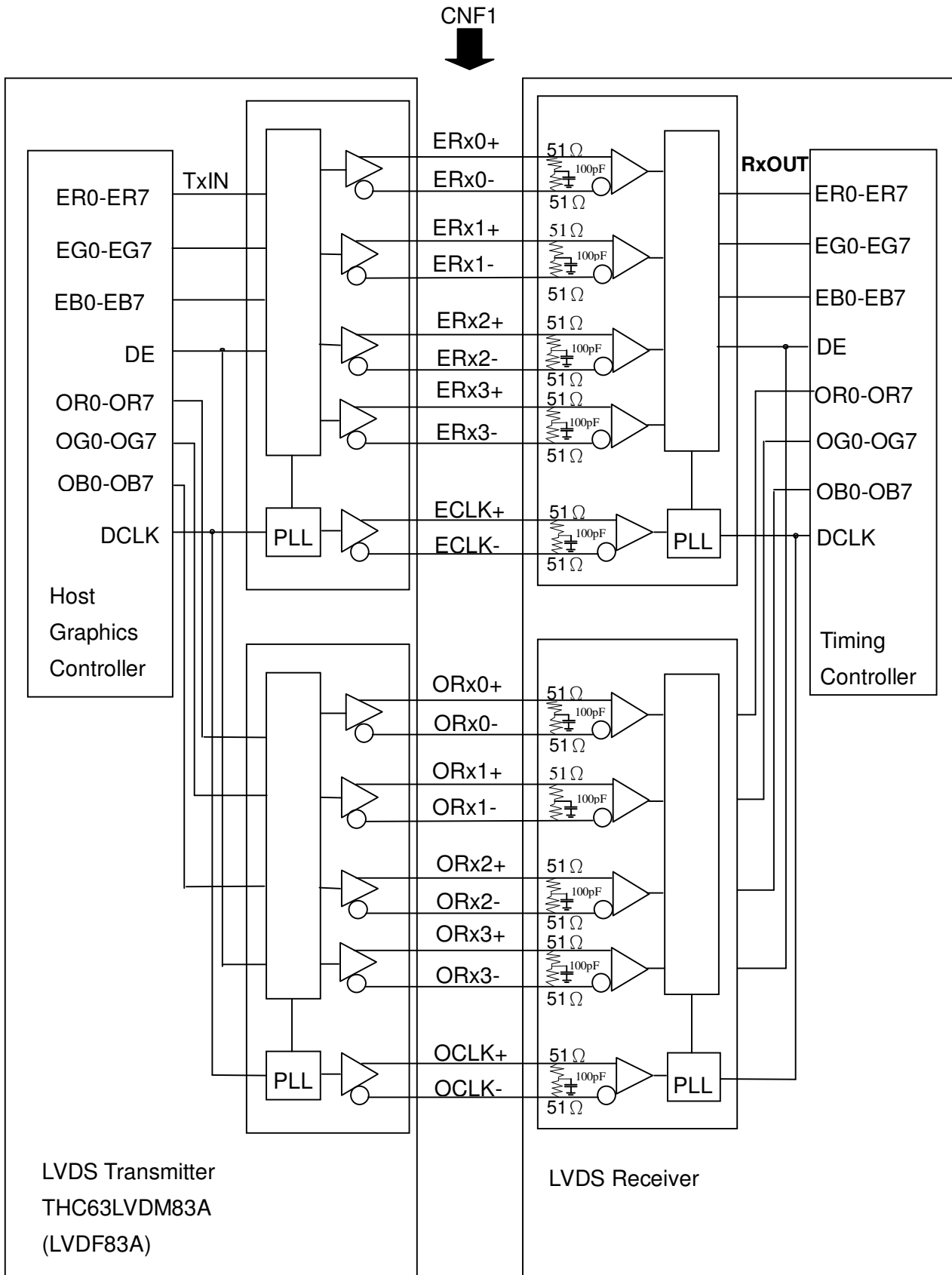
Pin No.	Symbol	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage

CN13(Header): 53261-1019 (Molex) or equivalent

Pin No.	Symbol	Description
1	CCFL Cold	CCFL Low voltage
2	CCFL Cold	CCFL Low voltage
3	CCFL Cold	CCFL Low voltage
4	CCFL Cold	CCFL Low voltage
5	CCFL Cold	CCFL Low voltage
6	CCFL Cold	CCFL Low voltage
7	CCFL Cold	CCFL Low voltage
8	CCFL Cold	CCFL Low voltage
9	CCFL Cold	CCFL Low voltage
10	CCFL Cold	CCFL Low voltage

Note (1) Floating of any control signal is not allowed.

5.4 BLOCK DIAGRAM OF INTERFACE



ER0~ER7 : Even pixel R data
EG0~EG7 : Even pixel G data
EB0~EB7 : Even pixel B data
OR0~OR7 : Odd pixel R data
OG0~OG7 : Odd pixel G data
OB0~OB7 : Odd pixel B data
DE : Data enable signal
DCLK : Data clock signal

- Notes: (1) The system must have the transmitter to drive the module.
- (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.
- (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is even pixel and the second pixel is odd pixel.

5.5 LVDS INTERFACE

	SIGNAL	TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT
		PIN	INPUT	Host	TFT-LCD	PIN	OUTPUT	
24bit	R0	51	TxIN0	TA OUT0+	Rx 0+	27	Rx OUT0	R0
	R1	52	TxIN1			29	Rx OUT1	R1
	R2	54	TxIN2			30	Rx OUT2	R2
	R3	55	TxIN3	TA OUT0-	Rx 0-	32	Rx OUT3	R3
	R4	56	TxIN4			33	Rx OUT4	R4
	R5	3	TxIN6			35	Rx OUT6	R5
	G0	4	TxIN7	TA OUT1+	Rx 1+	37	Rx OUT7	G0
	G1	6	TxIN8			38	Rx OUT8	G1
	G2	7	TxIN9			39	Rx OUT9	G2
	G3	11	TxIN12	TA OUT1-	Rx 1-	43	Rx OUT12	G3
	G4	12	TxIN13			45	Rx OUT13	G4
	G5	14	TxIN14			46	Rx OUT14	G5
	B0	15	TxIN15	TA OUT2+	Rx 2+	47	Rx OUT15	B0
	B1	19	TxIN18			51	Rx OUT18	B1
	B2	20	TxIN19			53	Rx OUT19	B2
	B3	22	TxIN20	TA OUT2-	Rx 2-	54	Rx OUT20	B3
	B4	23	TxIN21			55	Rx OUT21	B4
	B5	24	TxIN22			1	Rx OUT22	B5
	DE	30	TxIN26	TA OUT3+	Rx 3+	6	Rx OUT26	DE
	R6	50	TxIN27			7	Rx OUT27	R6
	R7	2	TxIN5			34	Rx OUT5	R7
	G6	8	TxIN10	TA OUT3-	Rx 3-	41	Rx OUT10	G6
	G7	10	TxIN11			42	Rx OUT11	G7
	B6	16	TxIN16			49	Rx OUT16	B6
	B7	18	TxIN17			50	Rx OUT17	B7
RSVD 1	25	TxIN23			2	Rx OUT23	Not connect	
RSVD 2	27	TxIN24			3	Rx OUT24	Not connect	
RSVD 3	28	TxIN25			5	Rx OUT25	Not connect	
	DCLK	31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK

R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD(reserved)pins on the transmitter shall be "H" or "L".

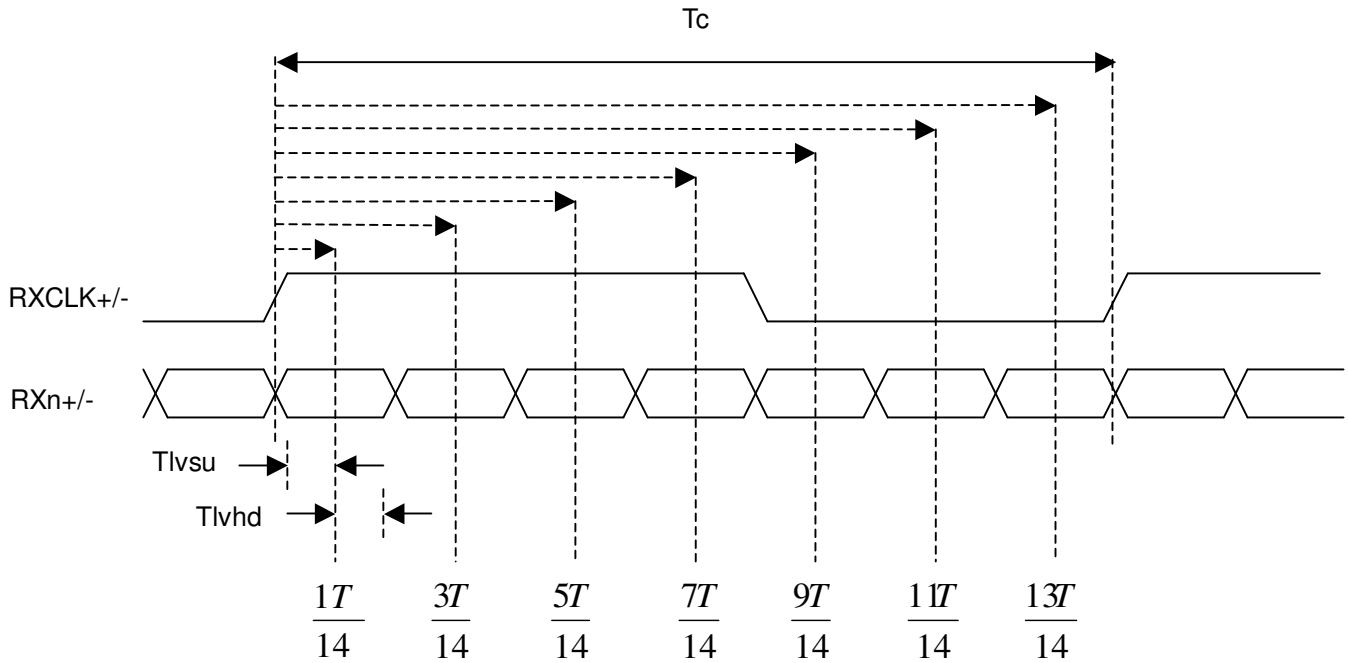
5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0		
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0		
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0		
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0		
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0		
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0		
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1		

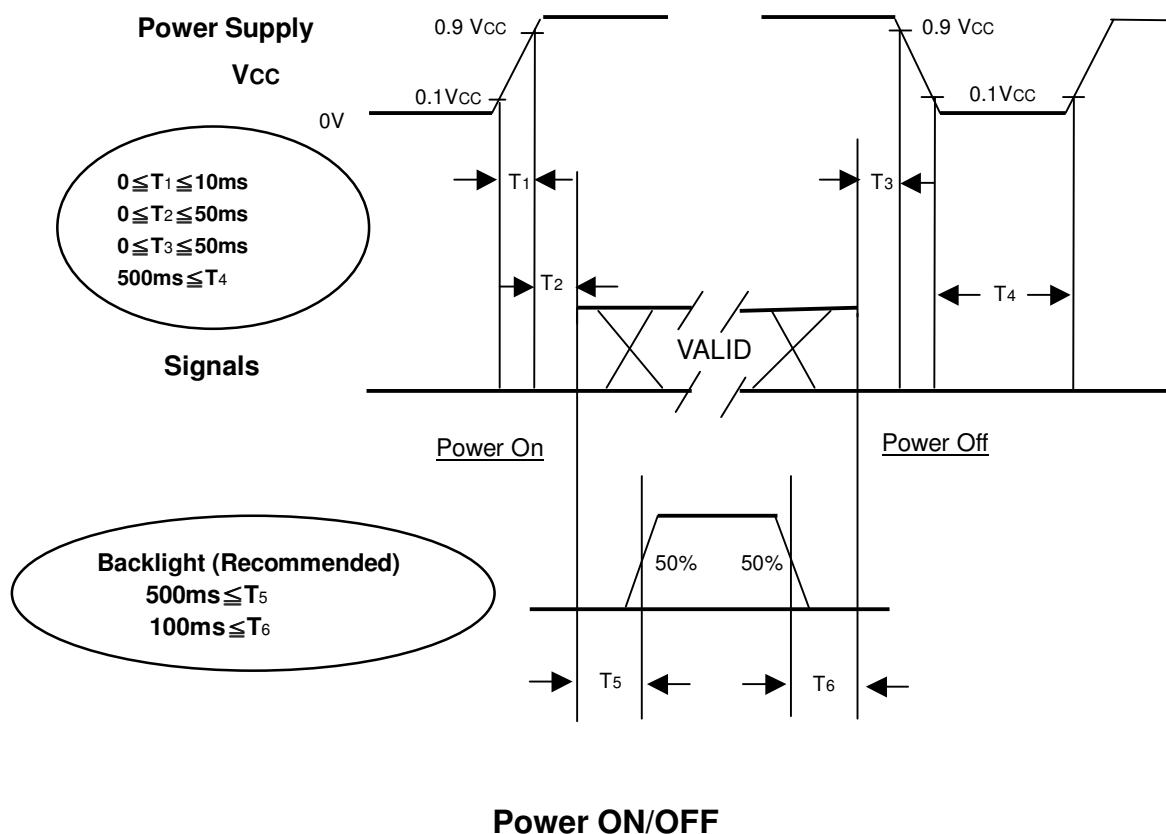
Note (1) 0: Low Level Voltage, 1: High Level Voltage

LVDS RECEIVER INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Note.

- (1) The supply voltage of the external system for the module input should follow the definition of Vcc.
- (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.
- (3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance.
- (4) T4 should be measured after the module has been fully discharged between power off and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I _L	4.8±0.5	mA
Oscillating Frequency (Inverter)	F _w	54±3	KHz
Frame Rate	F _r	60	Hz

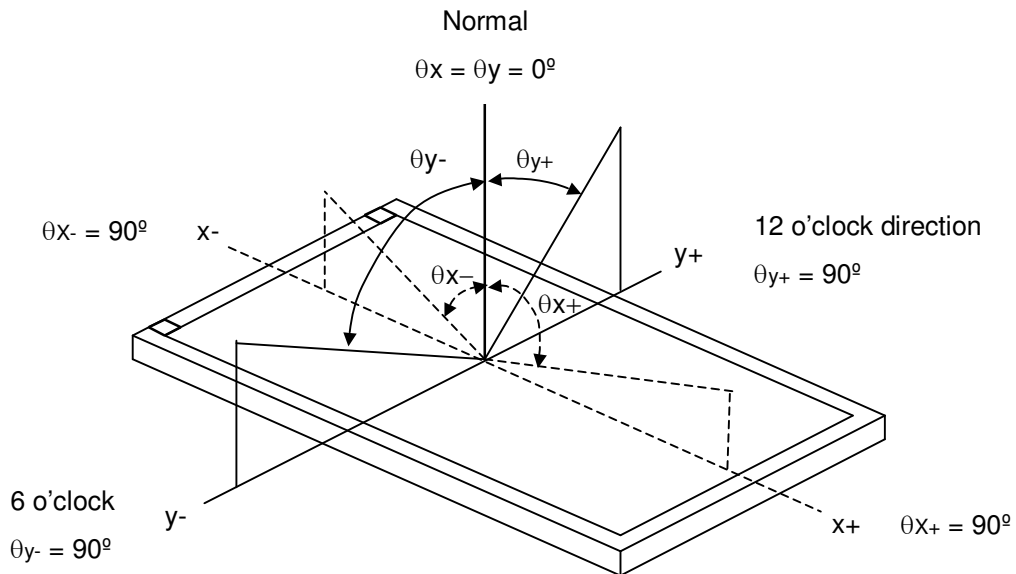
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Contrast Ratio	CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing Normal Angle	800	1000	-	-	(2)	
Response Time	Gray to Gray average		-	8	12	ms	(3)	
Center Luminance of White	L _C		500	600	-	cd/m ²	(4)	
Average Luminance of White	L _{Ave}		450	550	-	cd/m ²		
White Variation	δW		-	-	1.3	-	(7)	
Cross Talk	CT		-	-	4.0	%	(5)	
Color Chromaticity	Red		R _x	Typ. -0.03	0.650	Typ. +0.03	-	
			R _y		0.331			
	Green		G _x		0.270			
			G _y		0.590			
	Blue	B _x	0.142					
		B _y	0.068					
		White	W _x		0.285			
	W _y	0.293						
Viewing Angle	Horizontal	θ_{x+}	80	88	-	Deg.	(1)	
		θ_{x-}	80	88	-			
	Vertical	θ_{y+}	80	88	-			
		θ_{y-}	80	88	-			

Note (1) Definition of Viewing Angle (θ_x, θ_y):

Viewing angles are measured by EZ-Contrast 160R (Eldim)



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

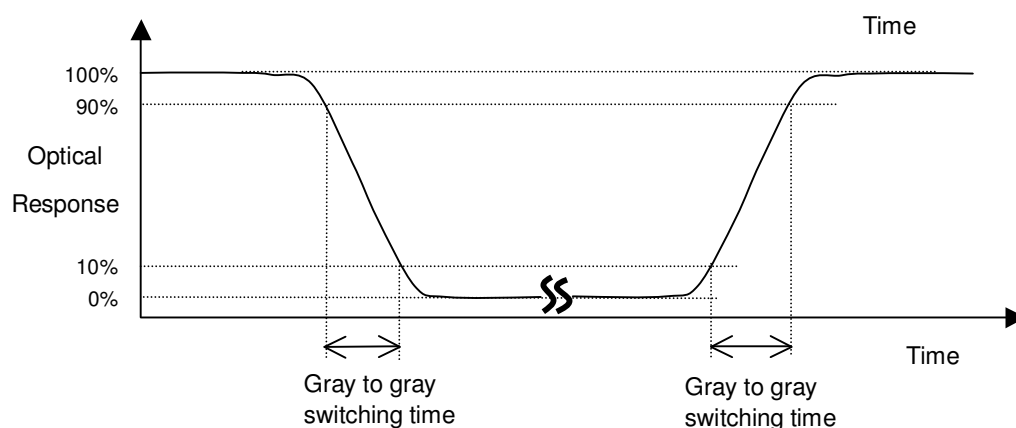
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

$$\text{CR} = \text{CR} (5)$$

CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

Note (3) Definition of Gray to Gray Switching Time:



The driving signal means the signal of gray level 0, 63, 127, 191, and 255.

Gray to gray average time means the average switching time of gray level 0, 63, 127, 191, 255 to each other.

Note (4) Definition of Luminance of White (L_C , L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

$$L_C = L(5)$$

$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

$L(x)$ is corresponding to the luminance of the point X at the figure in Note (7).

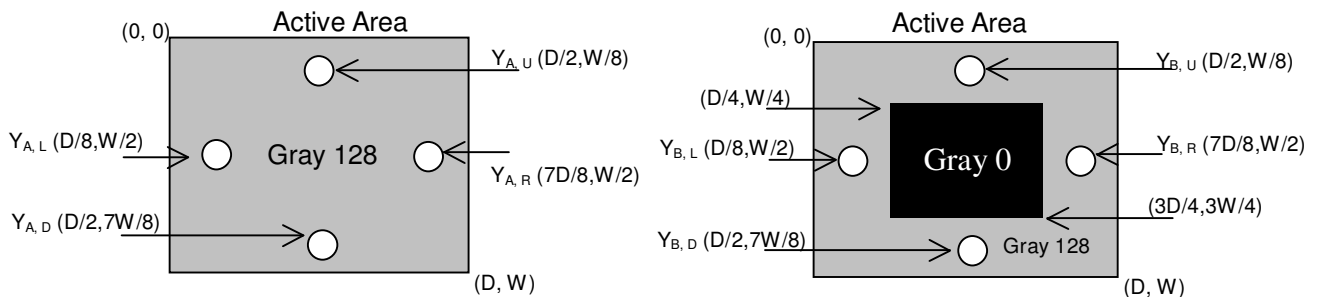
Note (5) Definition of Cross Talk (CT):

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

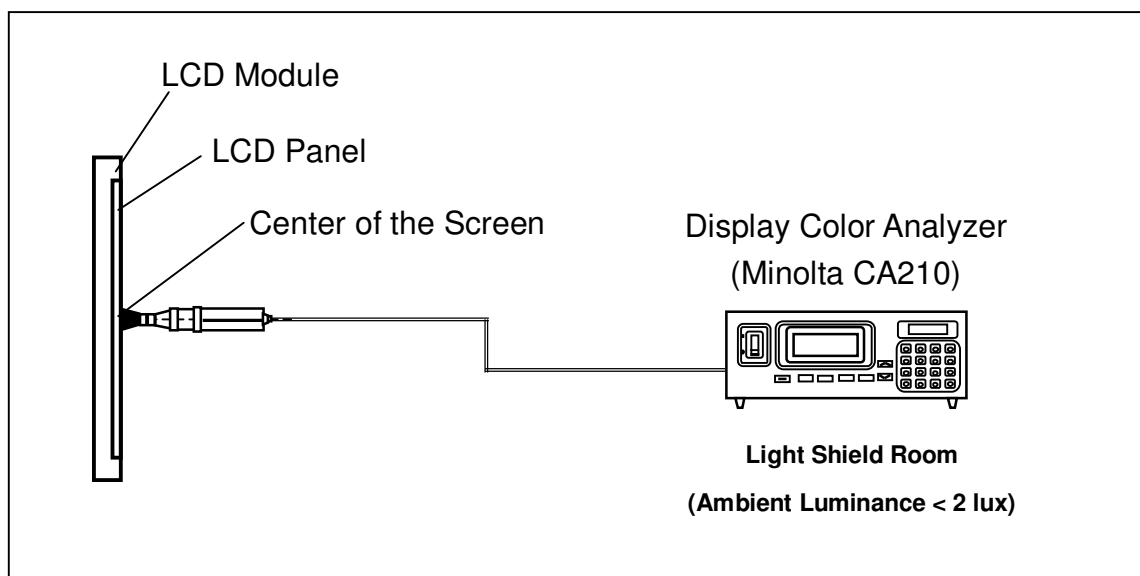
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



Note (6) Measurement Setup:

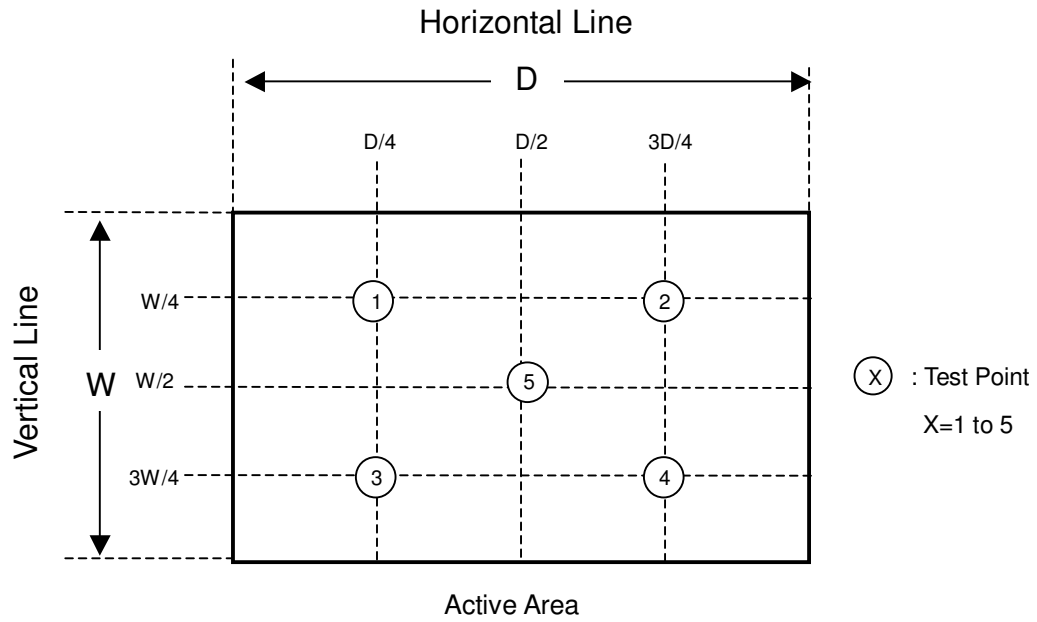
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

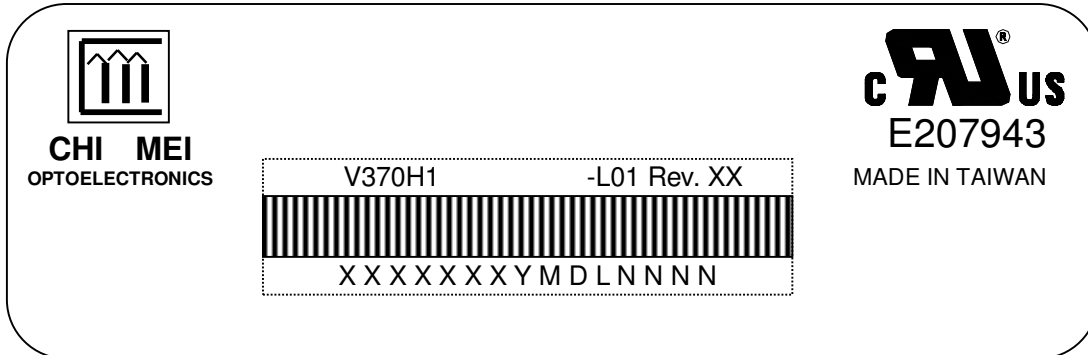
$$\delta W = \text{Maximum [L (1), L (2), L (3), L (4), L (5)]} / \text{Minimum [L (1), L (2), L (3), L (4), L (5)]}$$



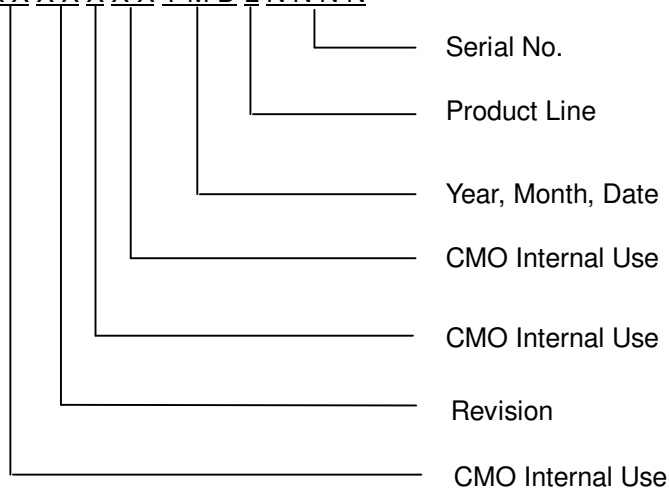
8. DEFINITION OF LABELS

8.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: V370H1-L01
- (b) Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.
- (c) Serial ID: XXXXXXXXYMDLNNNN



Serial ID includes the information as below:

- (a) Manufactured Date: Year: 0~9, for 2000~2009
 Month: 1~9, A~C, for Jan. ~ Dec.
 Day: 1~9, A~Y, for 1st to 31st, exclude I, O, and U.
- (b) Revision Code: Cover all the change
- (c) Serial No.: Manufacturing sequence of product
- (d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

9. PACKAGING

9.1 PACKING SPECIFICATIONS

- (1) 3 LCD TV modules / 1 Box
- (2) Box dimensions : 1048(L) X 345 (W) X 676 (H)
- (3) Weight : approximately 33Kg (3 modules per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

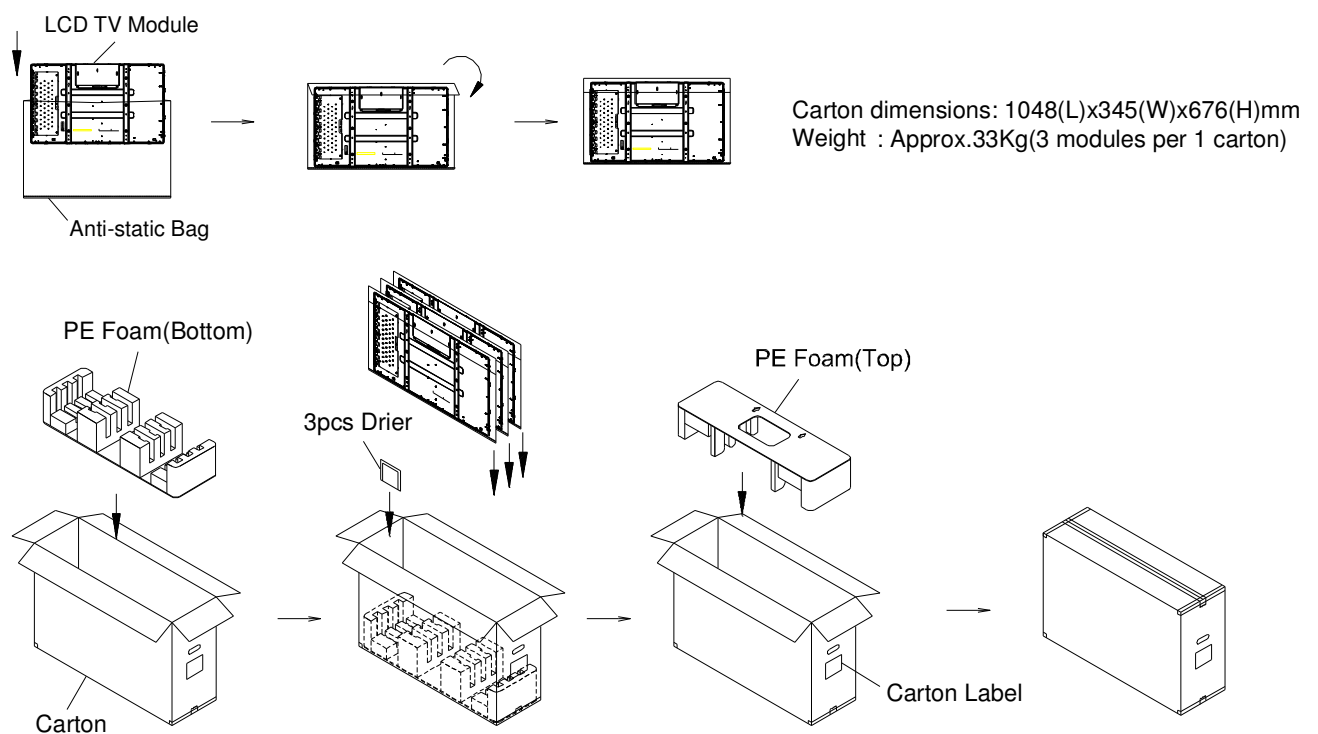


Figure.9-1 packing method

Corner Protector:L1350*50mm*50mm
Pallet:L1100*W1100*H145mm
Corrugated Fiberboard:L1100*W1100mm
Pallet Stack:L1100*W1100*H1500mm
Gross:218kg

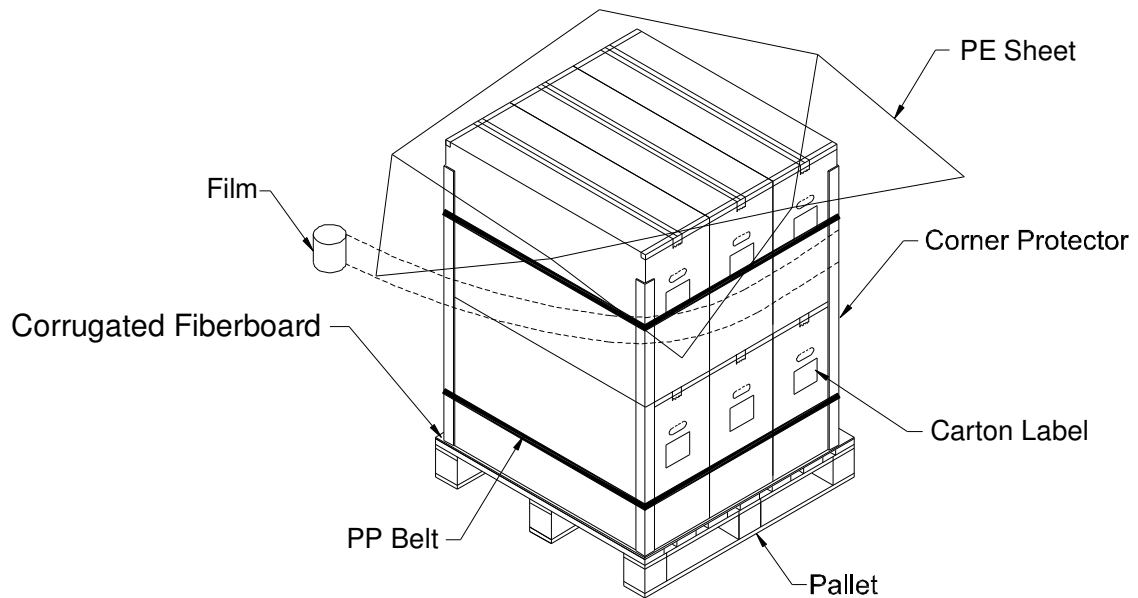


Figure. 9-2 Packing method

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.
- (4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- (5) Do not plug in or pull out the I/F connector while the module is in operation.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) Moisture can easily penetrate into LCD module and may cause the damage during operation.
- (9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.
- (10) When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

10.2 SAFETY PRECAUTIONS

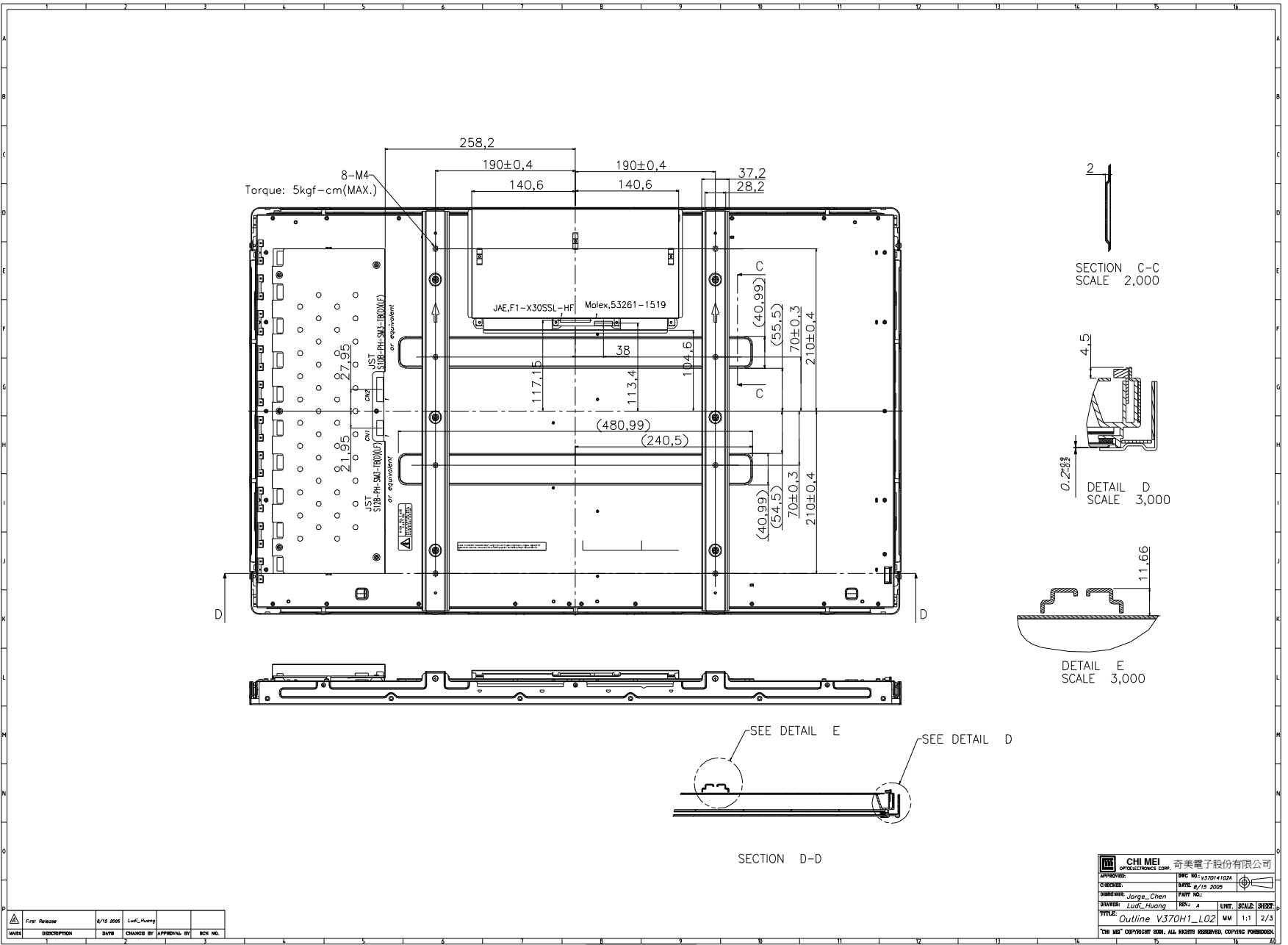
- (1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.



CHI MEI
OPTOELECTRONICS CORP.

Issued Date: Nov.30 2005
Model No.: V370H1 - L02

Approval

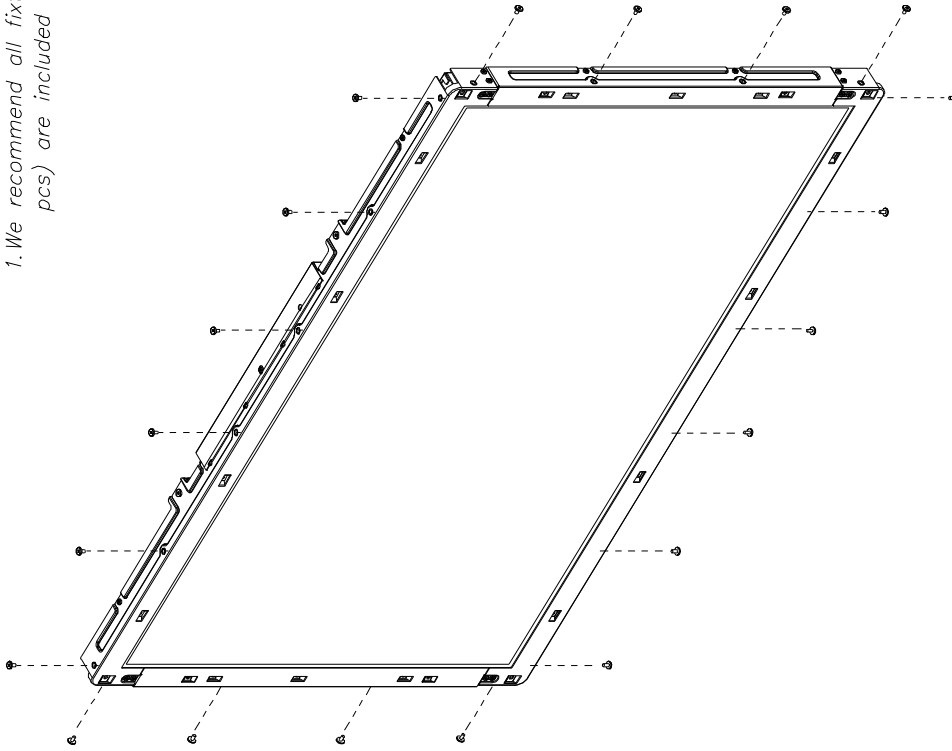


MARK	DESCRIPTION	DATE	CHANGE BY	APPROVAL BY	REV. NO.
	First Release	6/15 2005	Ludl_Huang		1

CHI MEI OPTOELECTRONICS CORP. 奇美電子股份有限公司	
APPROVED:	DWG NO: V370H1-102A
CHECKED: Jorgo_Chen	DATE: 6/15 2005
DRAWN: Ludl_Huang	PART NO:
	REV: A
	UNIT: MM
	SCALE: 1:1
	SHEET: 2/3
TITLE: Outline V370H1_L02	
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Note:

1. We recommend all fixture screws(20 pcs) are included while assembling.



CHI MEI 奇美電子股份有限公司	DATE: 11/30/2005
PROJECT: V370H1_L02	DATE: 11/30/2005
DESIGNER: Jangye Chen	DATE: 11/30/2005
DRAWN: Jangye Chen	DATE: 11/30/2005
CHECKER: Jangye Chen	DATE: 11/30/2005
APPROVER: Jangye Chen	DATE: 11/30/2005
TITLE: Outline V370H1_L02	NO. 1 of 3/3

DATE	DESCRIPTION	DATE	DESCRIPTION	DATE	DESCRIPTION