



SPECIFICATION For APPROVAL

- () Preliminary Specification
- () Final Specification

Title	18.1" SXGA TFT LCD
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BUYER NAME	
MODEL NAME	

SUPPLIER	LG LCD Inc.
MODEL NAME	LM181E1

SIGNATURE	DATE
_____ / _____	_____
_____ / _____	_____
_____ / _____	_____

APPROVED BY	DATE
_____ /G.Manager	_____
REVIEWED BY	
_____ /S.Engineer	_____
PREPARED BY	
_____ /S.Engineer	_____

Please return 1 copy for our confirmation with your signature and comments.

Product Engineering Dept.
LCD Division LG Electronics Inc.

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Record of revision

Date	Description	Note
1998,9,10 (Ver 2.1)	1 Input Voltage : 10.8 ~ 13.2V 11.3~12.5V 2.Change the note 3) 3.Change the power sequence 4.Add the humidity condition	5 Page 5 Page 16 Page 18 Page

1. General Description

The LG Electronics model LM181E1 LCD is a Color Active Matrix Liquid Crystal Display with an integral Cold Cathode Fluorescent Tube(CCFI) back light system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. This TFT-LCD has a 18.1 inch diagonally measured active display area with SXGA resolution(1024 vertical by 1280 horizontal pixel array). Each

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pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 8-bit gray scale signal for each dot, thus, presenting a palette of more than 16,581,375 colors.

LM181E1 has been designed to apply the interface method that enables low power, high speed low EMI. FPD-Link must be used as a LVDS(Low Voltage Differential Signaling) chip.

The LM181E1 LCD is intended to support applications where high brightness, wide viewing angle are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LM181E1 characteristics provide an excellent flat panel display for office automation products such as monitors.

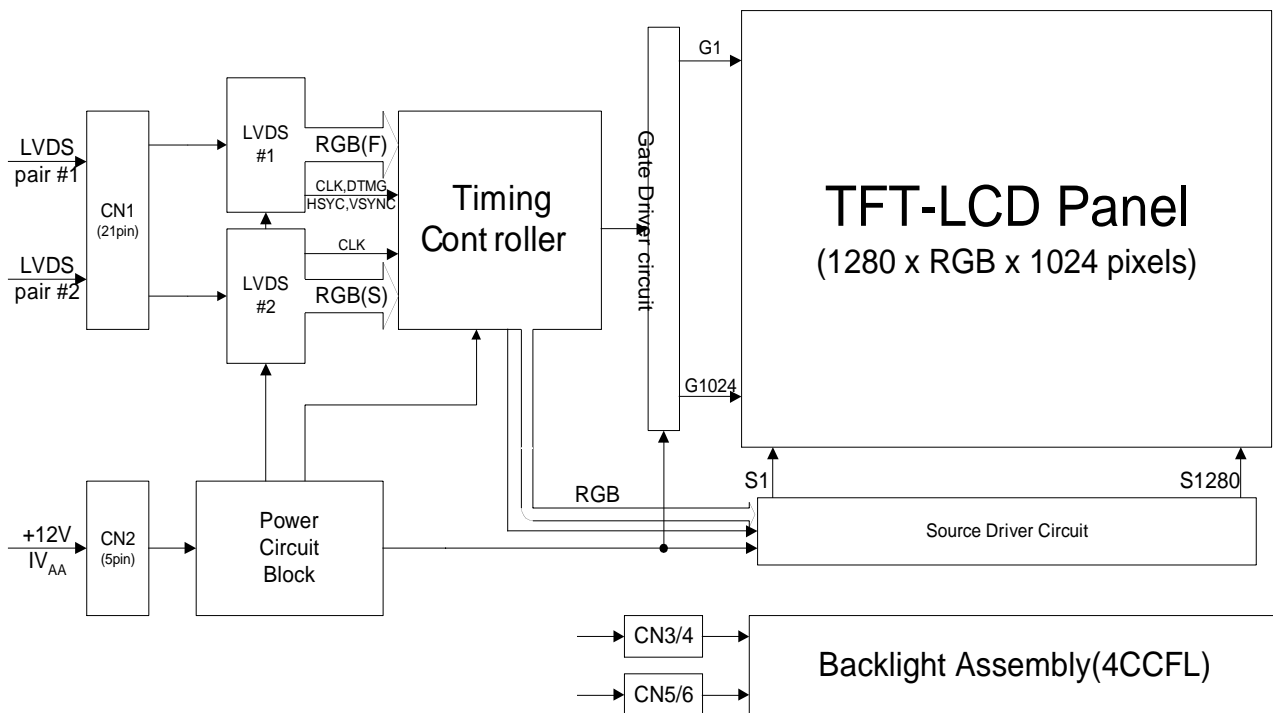


Figure 1. Block Diagram

General Display Characteristics

The following are general feature of the model LM181E1 LCD;

Active display area	18.1 inches(45.97cm) diagonal
Outsize dimensions	413.0W X 333.0H X 22.5T(typ)mm(Without Inverter)
Pixel pitch	0.2805 mm 0.2805 mm
Pixel format	1280 horiz. By 1024 vert. pixels
	RGB stripe arrangement
Color depth	8-bit, 16,581,375 colors
Display operating mode	transmissive mode, normally black
Surface treatments	hard coating(3H), anti-glare treatment of the front polarizer

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2. Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	symbol	Values		Units	Notes
		Min.	Max.		
Power Input Voltage	V_{AA}	0	+13.2	V_{DC}	at 25
Operating Temperature	T_{OP}	0	+50		25
Storage Temperature	T_{ST}	-10	+60		1

Note: 1. The Relative Humidity must not exceed 95% non-condensing at temperatures of 40 or less. At temperatures greater than 40, the wet bulb temperature must not exceed 39.

3. Electrical Specifications

The LM181E1 requires two power inputs. One is employed to power the LCD electronics and to drive the voltages to drive the TFT array and liquid crystal. The second input which powers the backlight CCFL, is typically generated by an inverter. The inverter is an external unit to the LCD.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Values			Units	Notes
		Min.	Typ.	Max.		
MODULE:						
Power Supply Input Voltage	V_{AA}	11.3	12.0	12.5	V_{DC}	1
Power Supply Input Current	I_{VAA}	-	0.65	1.2	A	1
Ripple/Noise	-	-	60	100	mV _{PP}	
Logic Input Level, High	V_{IH}	2.0	-	VCC	V_{DC}	2
Logic Input Level, Low	V_{IL}	$V_{SS}-0.2$	-	0.8	V_{DC}	2
Power Consumption	P_C	-	7.8	14.4	Watts	1
BACK LIGHT						
Back light Input voltage	V_{BL}	634	705	776	V_{RMS}	
Backlight Current	I_{BL}	-	8.0	8.5	mA	
Lamp Kick-Off Voltage	-	850	-	-	V_{RMS}	25
		1300	-	-	V_{RMS}	0
Operating Frequency	F_{BL}	30	-	60	KHz	
Power Consumption	P_{BL}	-	22.56	-	Watts	3
Life Time	-	15,000	20,000	-	Hours	4

Notes: 1. The current draw and power consumption specified is for 12.0 Vdc at 25 and fv at 60Hz. The LCM is displayed the 8-gray pattern for the typical current.

The maximum current measurement condition is the vertical 2-line white/black pattern(Input voltage :12.0 Vdc , Ambient temperature : 25, fv : 60Hz).

2. Logic levels are specified for 3.3Vdc at FPD-Link chips, transmitter & receiver. The values specified apply to all logic inputs to FPD-Link; Hsync, Vsync, clock, data signals, etc.

3. The backlight current consumption shown above does not include loss of external inverter. The power consumption is total of 4 CCFL.

4.The life time of backlight is half luminance than initial luminance.

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4. Optical Specifications

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes in a dark environment at 25 °C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0°.

The notes presents additional information concernening the speciffied charateristics.

Table 3. OPTICAL CHARACTERISTICS

Parameter	Symbol	Values			Units	Notes
		Min.	Typ.	Max.		
Contrast Ratio	CR	100	150	-	-	1
Surface Brightness, white	SB _{WH}	150	-	-	cd/m ²	2
Brightness Variation	SB _V	-	-	1.30	-	3
Response Time	Tr	-	50	100	msec	4
Rise Time	Tr _R	-	20	50		
Decay Time	Tr _D	-	30	50		
CIE Color Coordinates					-	-
Red	x _R	0.571	0.601	0.631		
	y _R	0.321	0.351	0.381		
Green	x _G	0.274	0.304	0.334		
	y _G	0.541	0.571	0.601		
Blue	x _B	0.118	0.148	0.178		
	y _B	0.104	0.134	0.164		
White	x _W	0.285	0.315	0.345		
	y _W	0.333	0.363	0.393		
Viewing Angle					degree,	5
x axis, right (=0°)		60	70	80		
x axis, left(=180°)		60	70	80		
y axis, up(=90°)		60	70	80		
y axis, down (=270°)		60	70	80		
Halt Luminance Angle					degree,	6
x axis, right (=0°)		45	-	-		
x axis, left(=180°)		45	-	-		
y axis, up(=90°)		45	-	-		
y axis, down (=270°)		45	-	-		
Cross talk	-	-	-	4	%	7
Flicker	-	-	-	-20	dB	8
Gamma value	-	-	-	-	-	9

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Notes 1. Contrast Ratio (CR) is defined mathematically as:

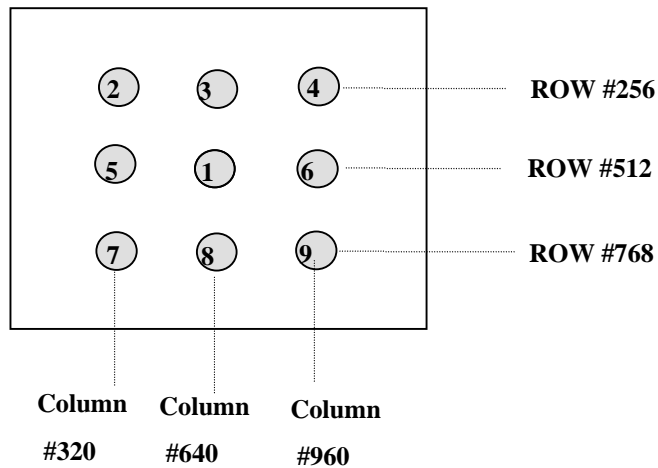
$$CR = \frac{\text{(Surface Brightness with all white pixels)}}{\text{(Surface Brightness with all black pixels)}}$$

2. Surface brightness is the average of 5 measurement across the LCD surface 50cm from the surface with all pixels displaying white. The photometer is CA-110, the current of lamp is 8.5mA

$$SB_{WH} = \frac{(B1 + B2 + B4 + B7 + B9)}{5}$$

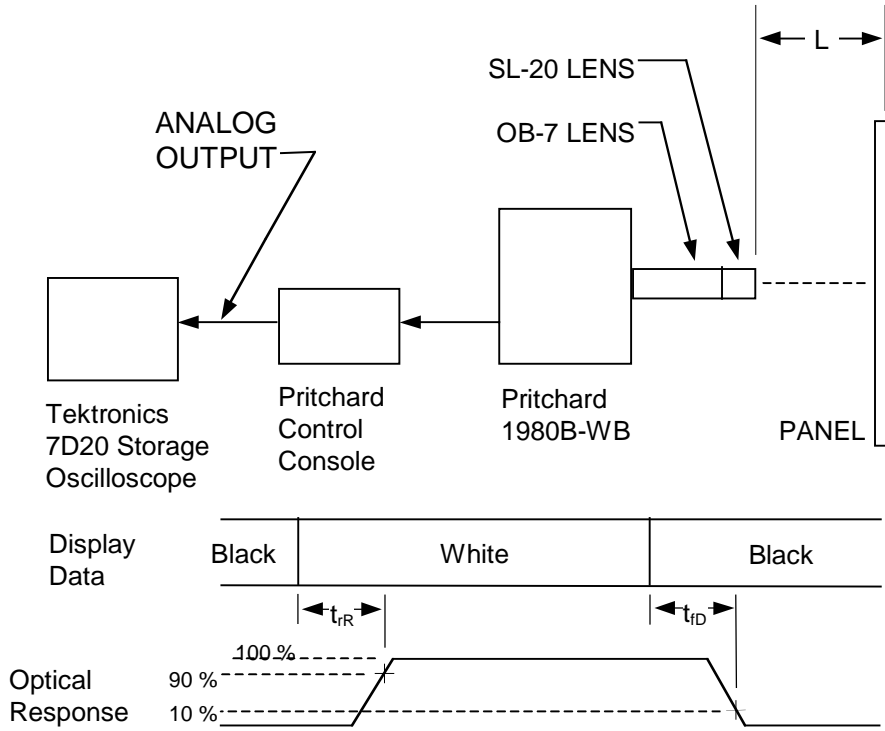
3. The variation in surface brightness, SB_V is determined by measuring B_{ON} at each test position 1 through 9, and then dividing the maximum B_{ON} - minimum B_{ON} by the average B_{ON}.

$$SB_V = \frac{\text{Maximum (B 1, B2, B4, B7, B9)}}{\text{Minimum (B 1, B2, B4, B7, B9)}}$$



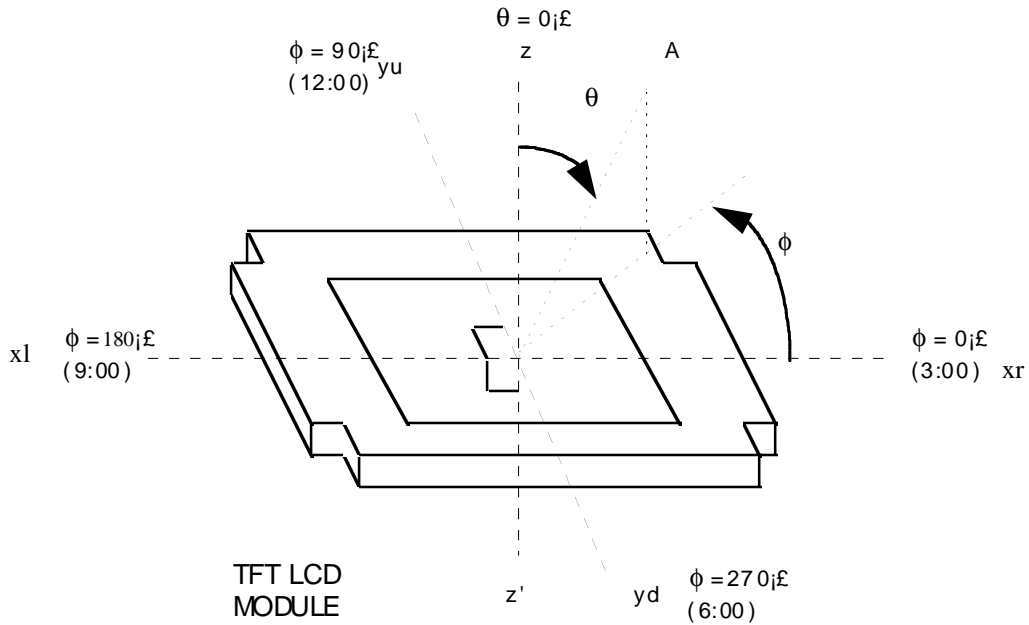
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4. Response time is the time required for the display to transition from white to black (Decay Time, T_{rD}) and from black to white (Rise Time, T_{rR}). The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white". The reference of measurement is the line of data transition. The criteria of response time is set when input signal of measured position transite white and black.



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5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.



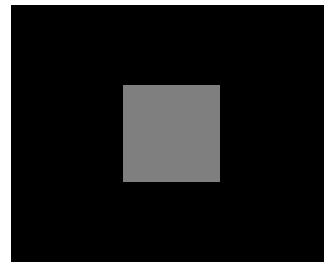
6. Half Luminance angle is defined as the up, down, left, and right angular boundaries at which the luminance value is 50% of the luminance value measured on-axis. It is measured at the center position with all white image.

7. Cross talk shall be measured at the center position. (Window size : 100 x 100 pixels)

$$\text{Crosstalk Ratio} = \frac{(\text{Brightness at pattern A} - \text{Brightness at pattern B})}{\text{Brightness at pattern A}} \leq 10\%$$



(Background : Mid-gray)
Pattern A

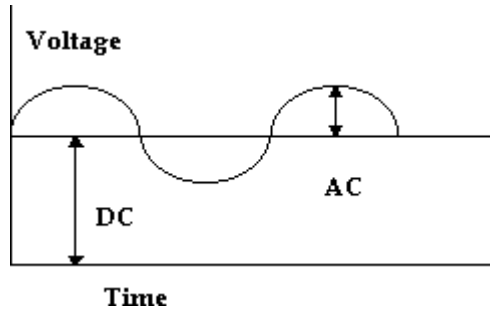


(Background : Black, Window: Mid-gray)
Pattern B

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8. Flicker shall be measured at the center location.

Test pattern : Pixel pattern
 Background RGB gray(0, 0, 0)
 Foreground RGB gray(127, 127, 127)



9. Gamma value

n	Gs(S)	Relative Brightness (%)			Remark
		Min.	Typ.	Max.	
0	0	0.2	0.4	0.7	
1	31	2.0	3.1	4.2	
2	63	5.4	7.5	9.2	
3	95	10.4	13.	16.9	
4	127	16.8	21.2	25.6	
5	159	25.3	31.6	37.4	
6	191	35.7	46.1	55.2	
7	223	58.9	68.2	78.5	
8	255	-	100	-	

5. Interface Connections

Interface chip must be used LVDS, part No. DS90CF383MTD made by National Semiconductor. Or used the compatible interface chips(TI,Thine).

This LCD employs six interface connections, a 21 pin connector is used for the module electronics, a five pin connector is used for the module power(+12V), and four connector, a two pin connector, is used for the integral backlight system.

The electronics interface connector is a model FI-WE21PB-VF manufactured by JAE. The pin configuration for the connector is shown in the table 4.

Table 4. MODULE CONNECTOR PIN CONFIGURATION(for the LVDS signal)

Pin	Symbol	Description	Notes
1	FR3P	Plus Signal of Odd Channel 3 (LVDS)	} First Data
2	FR3M	Minus Signal of Odd Channel 3 (LVDS)	
3	FCLKINP	Plus Signal of Odd Clock Channel (LVDS)	
4	FCLKINM	Minus Signal of Odd Clock Channel (LVDS)	
5	FR2P	Plus Signal of Odd Channel 2 (LVDS)	
6	FR2M	Minus Signal of Odd Channel 2 (LVDS)	
7	FR1P	Plus Signal of Odd Channel 1 (LVDS)	
8	FR1M	Minus Signal of Odd Channel 1 (LVDS)	
9	FR0P	Plus Signal of Odd Channel 0 (LVDS)	
10	FR0M	Minus Signal of Odd Channel 0 (LVDS)	
11	SR3P	Plus Signal of Even Channel 3 (LVDS)	} Second
12	SR3M	Minus Signal of Even Channel 3 (LVDS)	
13	SCLKINP	Plus Signal of Even Clock Channel (LVDS)	
14	SCLKINM	Minus Signal of Even Clock Channel (LVDS)	
15	SR2P	Plus Signal of Even Channel 2 (LVDS)	
16	SR2M	Minus Signal of Even Channel 2 (LVDS)	
17	SR1P	Plus Signal of Even Channel 1 (LVDS)	
18	SR1M	Minus Signal of Even Channel 1 (LVDS)	
19	SR0P	Plus Signal of Even Channel 0 (LVDS)	
20	SR0M	Minus Signal of Even Channel 0 (LVDS)	
21	NC	Not Connect	

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The module power connector is a model B5B-ZR-SM3-IF manufactured by JST. The pin configuration for the connector is shown in the table 5.

Table 5. POWER CONNECTOR PIN CONFIGURATION

Pin	Symbol	Description	Notes
1	GND	Ground	1
2	GND	Ground	
3	NC	Not Connect	
4	IV _{AA}	Supply voltage for LCD module	2
5	IV _{AA}	Supply voltage for LCD module	

- Notes: 1. All GND(ground) pins should be connected together and to Vss which should also be connected to the LCD's metal frame.
 2. All IV_{AA}(power input) pins should be connected together.

The backlight interface connector is a model BHSR-02VS-1, manufactured by JST. The mating connector part number is SM02B-BHsS-1 or equivalent. The pin configuration for the connector is shown in the table 6.

Table 6. BACKLIGHT CONNECTOR PIN CONFIGURATION

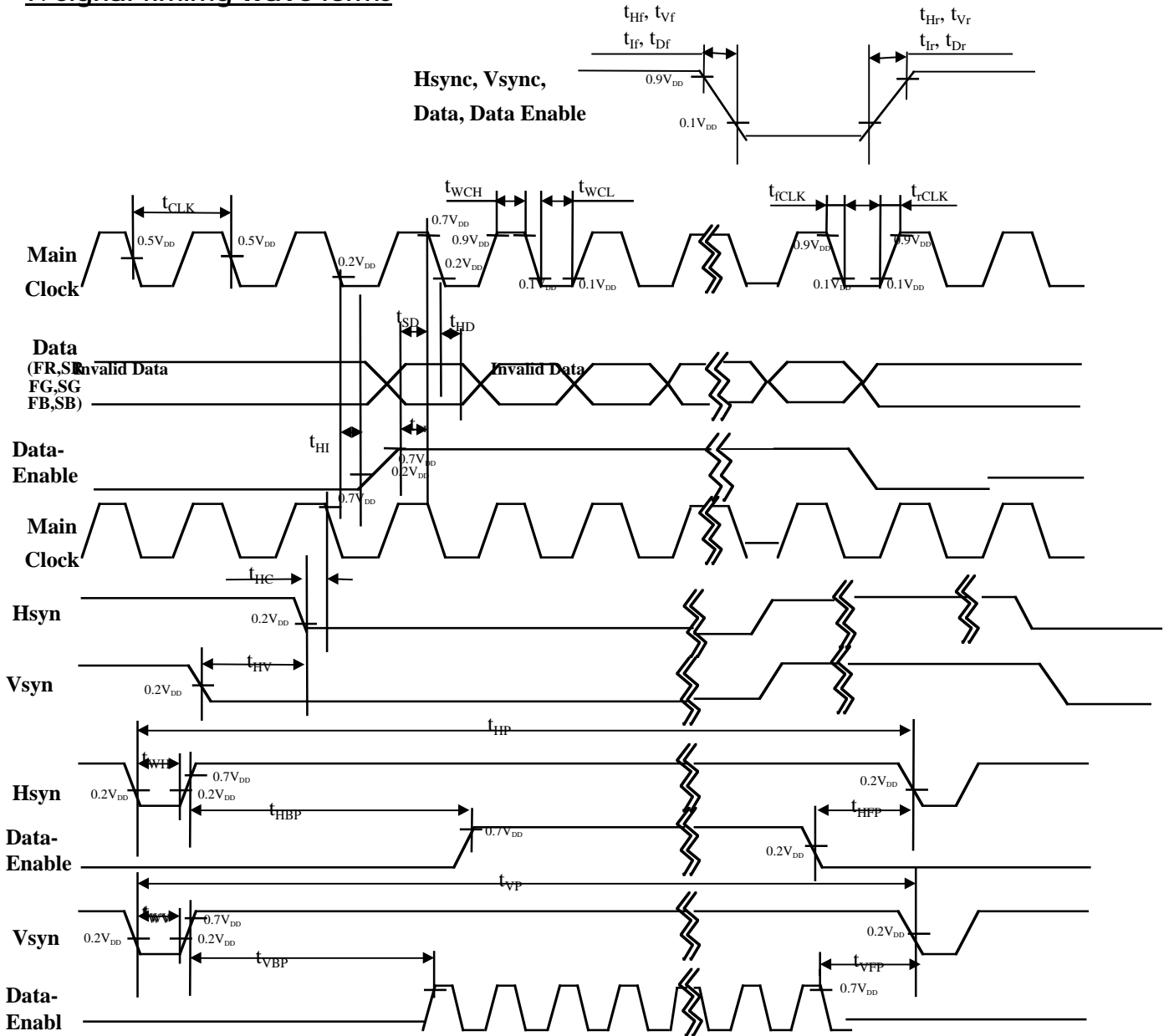
Pin	Symbol	Description	Notes
1	HV	Lamp power input	1
2	LV	Ground	2

- Notes: 1. The input power terminal is colored pink. Ground pin color is white.
 2. The backlight ground should be common with Vss.

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6. Signal Timing Specification(Between FPD-Link & Timing Controller)

Parameter		Symbol	Value			Units	Notes
			Min.	Typ.	Max.		
Main Clock	Frequency	$f_{CLK}(=1/t_{CLK})$	42.5	54.0	54.0	MHz	Dclk : 85~108MHz
	High duration	t_{wCH}	$0.4 t_{CLK}$	$0.5 t_{CLK}$	$0.6 t_{CLK}$	ns	
	Low duration	t_{wCL}	$0.4 t_{CLK}$	$0.5 t_{CLK}$	$0.6 t_{CLK}$	ns	
	Rise Time	t_{rCLK}	-	-	2.3	ns	
	Fall Time	t_{fCLK}	-	-	1.4	ns	
Data	Set-up duration	t_{SD}	5.0	-	-	ns	for f_{CLK}
	Hold duration	t_{HD}	5.0	-	-	ns	for f_{CLK}
	Rise Time	t_{Dr}	-	-	4.5	ns	$C_L = 15pF$
	Fall Time	t_{Df}	-	-	2.1	ns	$C_L = 15pF$
Hsync	Period	t_{HP}	12.6	15.63	-	clock	
			680	844	-		
	Pulse Width	t_{WH}	8	56	-	clock	
	Rise/Fall Time	t_{Hr}, t_{Hf}	-	-	5	ns	
Vsync	Period	t_{VP}	16.661	16.661	16.661	msec	$f_V=60Hz$
			1032	1066	-	lines	
	Pulse Width	t_{WV}	2	3	-	lines	
	Rise/Fall Time	t_{Vr}, t_{Vf}	-	-	10	ns	
Data Enable	Set-up duration	t_{SI}	5	-	-	ns	for f_{CLK} for f_{CLK}
	Hold duration	t_{HI}	5	-	-	ns	
	Horizontal Back Porch	t_{HBP}	12	124	-	clock	
	Horizontal Active		640	640	640	clock	
	Horizontal Front porch	t_{HFP}	8	24	-	clock	
	Vertical Back Porch	t_{VBP}	1	38	-	lines	
	Vertical Active		1024	1024	1024	lines	
	Vertical Front porch	t_{VFP}	1	1	-	lines	
Rise/Fall Time	t_{Ir}, t_{If}	-	-	5	ns		
Hsync- Clock phase difference		t_{HC}	$t_{CLK}-10$	-	t_{wCL}	ns	
Hsync-Vsync phase difference		t_{HV}	-	-	$t_{HP}-t_{WH}$	ns	

7. Signal Timing Wave forms



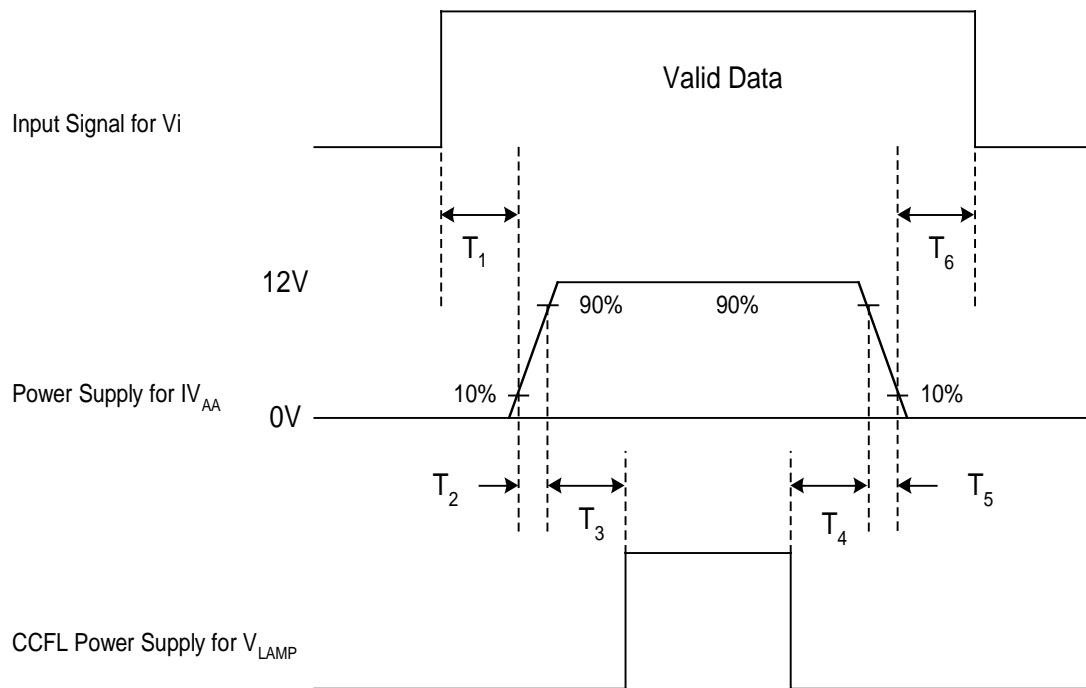
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8. Color Input Data Reference

The brightness of each primary color(red, green and blue) is based on the 8-bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 7. COLOR DATA REFERENCE

Color		Input Color Data																							
		Red								Green								Blue							
		MSB				LSB				MSB				LSB				MSB		LSB					
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red(000) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(001)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(002)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255) Bright	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green(000)Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(002)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
Green(255)Bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Blue	Blue(000) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(002)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255) Bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

9. Power Sequence



* Set 0 Volt < $IV_{AA}(t) < V_i(t)$

Here $V_i(t)$, $IV_{AA}(t)$ indicate the transitive state of V_i , IV_{AA} when power supply is turned ON or OFF

* T₁, T₆ : 50 ms ~ 300 ms.

* T₂, T₅ : 20 ms .

* T₃, T₄ : 100 ms ~ 200 ms.

Notes: 1. Please avoid floating state of interface signal at invalid period.

2. When the interface signal is invalid, be sure to pull down the power supply for LCD IV_{CC} to 0V.

3. BackLight Inverter power must be turn on after power supply for logic and interface signal are valid.

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10. Mechanical Characteristics

The chart below provides general mechanical characteristics for the model LM181E1 LCD. In addition, the figure 2 is a detailed mechanical drawing of the LCD. Note that dimension are given for reference purposes only.

Outside dimensions:	Width	413.0mm(TYP.)
	Height	333.0mm(TYP.)
	Thickness	22.5mm(TYP.)
Active Display area	Width	359.040mm
	Height	287.232mm
Weight (approximate)	3000 gram (Max.)	

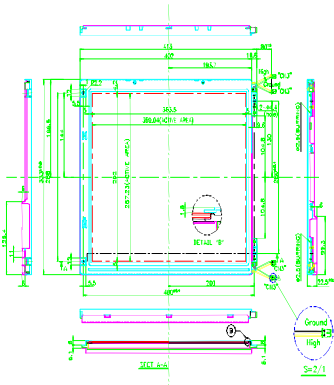


Figure 2. Detailed mechanical drawing

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11. Reliability

No.	Test ITEM	Conditions
1	High temperature storage test	Ta = 60 240h
2	Low temperature storage test	Ta = -10 240h
3	High temperature operation test	Ta = 50 240h
4	Low temperature operation test	Ta = 0 240h
5	Altitude	Operating : 12,000ft Storage : 40,000ft
6	Humidity Condition	Operating : 20%~80% RH Non-Operating : 5~95% RH
7	Shock & Vibration test	Operating
		Non-operating
8	ESD test (non-operating)	Condition : 150 330 Terminal : 200V Chassis : 10

{Result Evaluation Criteria}

There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.



12. Cosmetic(TBD)

13. PRECAUTIONS

Please pay attention to the followings when you use this TFT/LCD module with Back-light unit.

- 1) You must mount Module using mounting holes arranged in 4 corners.
- 2) Be sure to turn off the power when connecting or disconnecting the circuit.
- 3) Note that the polarizers are easily damaged. Pay attention not to scratch or press this surface with any hard object.

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- 4) When the LCD surface become dirty, please wipe it off with a soft material.
(ie.cotton ball)
- 5) Protect the module from the ESD as it may damage the electronic circuit (C-MOS).
Make certain that treatment person's body are grounded through wrist bend.
- 6) Do not disassemble the module and be careful not to incur a mechanical shock that might occur during installation. It may cause permanent damage.
- 7) Do not leave the module in high temperatures, Particularly in areas of high humidity for a long time.
- 8) The module not be expose to the direct sunlight.
- 9) Avoid contact with water as it may a short circuit within the module.

Product Specification
A. Appendix (DS90CF383 Pin Description - FPD Link Transmitter)

Pin #	Pin Name	Require Signal	Pin #	Pin Name	Require Signal
1	VCC	Power supply for TTL input	29	GND	Ground pin for TTL
2	D5	TTL Input (R7)	30	D26	TTL Input (DE)
3	D6	TTL Input (R5)	31	TxCLKIN	TTL level clock input
4	D7	TTL Input (G0)	32	PWR DWN	Power down input
5	GND	Ground pin for TTL	33	PLL GND	Ground for PLL
6	D8	TTL Input (G1)	34	PLL VCC	Power supply for PLL
7	D9	TTL Input (G2)	35	PLL GND	Ground for PLL
8	D10	TTL Input (G6)	36	LVDS GND	Ground for LVDS
9	VCC	Power supply for TTL input	37	TxOUT3+	Positive LVDS differential data output 3
10	D11	TTL Input (G7)	38	TxOUT3-	Negative LVDS differential data output 3
11	D12	TTL Input (G3)	39	TxCLKOUT +	Positive LVDS differential clock output
12	D13	TTL Input (G4)	40	TxCLKOUT-	Negative LVDS differential clock output
13	GND	Ground for TTL	41	TxOUT2+	Positive LVDS differential data output 2
14	D14	TTL Input (G5)	42	TxOUT2-	Negative LVDS differential data output 2
15	D15	TTL Input (B0)	43	LVDS GND	Ground for LVDS
16	D16	TTL Input (B6)	44	LVDS VCC	Power supply for LVDS
17	VCC	Power supply for TTL input	45	TxOUT1+	Positive LVDS differential data output 1
18	D17	TTL Input (B7)	46	TxOUT1-	Negative LVDS differential data output 1
19	D18	TTL Input (B1)	47	TxOUT0+	Positive LVDS differential data output 0
20	D19	TTL Input (B2)	48	TxOUT0-	Negative LVDS differential data output 0
21	GND	Ground for TTL	49	LVDS GND	Ground for LVDS
22	D20	TTL Input (B3)	50	D27	TTL Input (R6)
23	D21	TTL Input (B4)	51	D0	TTL Input (R0)
24	D22	TTL Input(R5)	52	D1	TTL Input (R1)
25	D23	TTL Input(RSVD)	53	GND	Ground for TTL
26	VCC	Power supply for TTL input	54	D2	TTL Input (R2)
27	D24	TTL Input (HSYNC)	55	D3	TTL Input (R3)
28	D25	TTL Input (VSYNC)	56	D4	TTL Input (R4)