





TFT LCD Approval Specification

MODEL NO.: N141XB -L07
(Lead Free Model)

Customer : _____

Approved by : _____

Note :

Liquid Crystal Display Division	
QRA Division.	OA Head Division.
Approval	Approval
	

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 1.0	Aug. 13. '04	All	All	Preliminary specification first issued.
Ver 1.1	Oct. 04. '04	1	Cover	Add " Lead Free Model " description
		4	1.2	Add " lead free model " description
			1.5	Modify the weight spec to with inverter Without inverter 420 typ / 430 max → With inverter 430 typ / 440max
Ver 2.0	Nov. 03. '04	7	3.1	Modify Power Supply Current Max value White 450 → 380 , Black/Vertical Stripe 500 → 480
		14~17	5.5	Update EDID Data for 256 steps inverter
		22	6.4	Update Brightness Control SM-BUS Table for 256 steps inverter

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N141XB -L07 is a 14.1" TFT Liquid Crystal Display module with single CCFL Backlight unit and 30 pins LVDS interface and inverter. This module supports 1024 x 768 XGA mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction.

1.2 FEATURES

- With inverter
- Thin and light weight
- XGA (1024 x 768 pixels) resolution
- DE (Data Enable) only mode
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 1 pixel/clock
- SPWG (Standard Panel Working Group) Style B compatible and lead free model

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATIONS

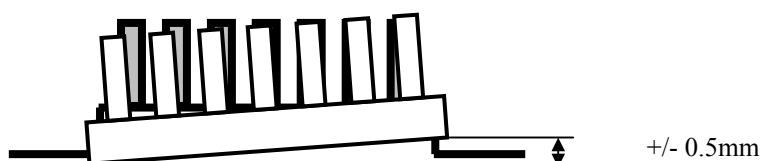
Item	Specification	Unit	Note
Active Area	285.7 (H) x 214.3 (V) (14.1" diagonal)	mm	(1)
Bezel Opening Area	288.9 (H) x 217.5 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1024 x R.G.B. x 768	pixel	-
Pixel Pitch	0.279 (H) x 0.279 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hardness (3H), Anti-glare (Haze 25)	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size (without inverter)	Horizontal(H)	298.5	299.0	299.5	mm	(1)
	Vertical(V)	227.5	228.0	228.5	mm	
	Depth(D)	-	5.2	5.5	mm	
Weight (Panel with inverter)		-	430	440	g	-
I/F connector mounting position		The mounting inclination of the connector makes the screen center within $\pm 0.5\text{mm}$ as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

(2) Connector mounting position



2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Storage Humidity	H _{ST}	5	95	%RH	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)
Operating Ambient Humidity	H _{OP}	8	95	%RH	(1)
Shock (Non-Operating)	S _{NOP}	-	50 18 220 2	G ms G ms	(3), (4), (5)
Vibration (Non-Operating)	V _{NOP}	-	1.5 10-200	G Hz	(4), (5)

Note (1) (a) 95 %RH Max. ($T_a \leq 40$ °C).

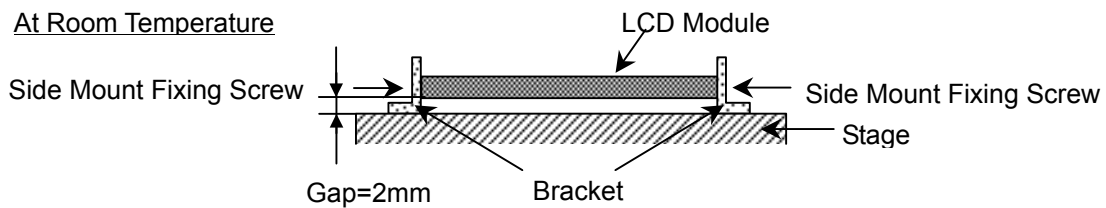
(b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40$ °C).

(c) No condensation .

Note (2) The temperature of panel surface should be 0 °C Min. and 50 °C Max.

Note (3) Condition for 50G 18ms is Rectangle Wave. Condition for 220G 2ms is Half Sine Wave.

Note (4) The fixing condition is shown as below:



Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V _{CC}	-0.3	+4.0	V	(1)
Logic Input Voltage	V _{IN}	-0.3	V _{CC} +0.3	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V _L	-	2.5K	V _{RMS}	(1), (2), I _L = (6.0) mA
Lamp Current	I _L	-	6.5	mA _{RMS}	
Lamp Frequency	F _L	-	80	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to Section 3.2 for further information).

3. ELECTRICAL CHARACTERISTICS

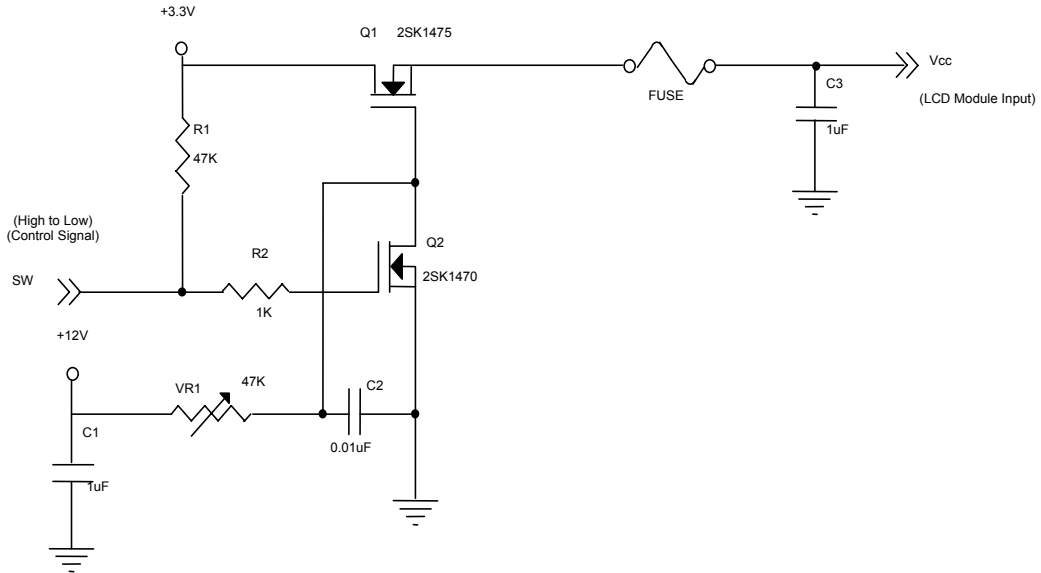
3.1 TFT LCD MODULE

Ta = 25 ± 2 °C

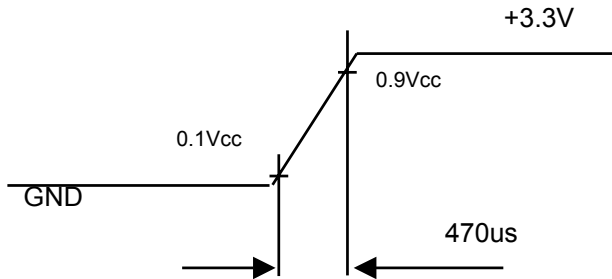
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage	V _{CC}	3.0	3.3	3.6	V	-
Ripple Voltage	V _{RP}	-	-	100	mV	-
Rush Current	I _{RUSH}	-	-	1.5	A	(2)
Power Supply Current	White	-	350	380	mA	(3)a
	Black	-	450	480	mA	(3)b
	Vertical Stripe	-	450	480	mA	(3)c
Differential Input Voltage for LVDS Receiver Threshold	"H" Level	V _{IH}	-	+100	mV	-
	"L" Level	V _{IL}	-100	-	mV	-
Terminating Resistor	R _T	-	100	-	Ohm	-

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470us



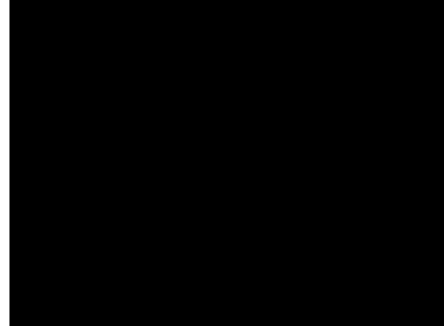
Note (3) The specified power supply current is under the conditions at $V_{cc} = 3.3\text{ V}$, $T_a = 25 \pm 2\text{ }^\circ\text{C}$, DC Current and $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



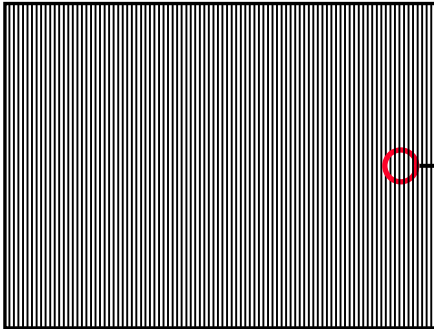
Active Area

b. Black Pattern

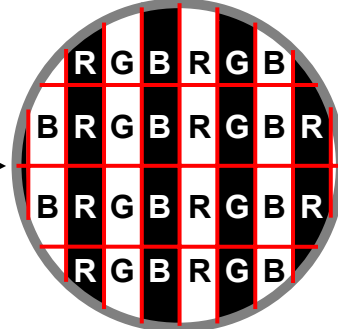


Active Area

c. Vertical Stripe Pattern



Active Area

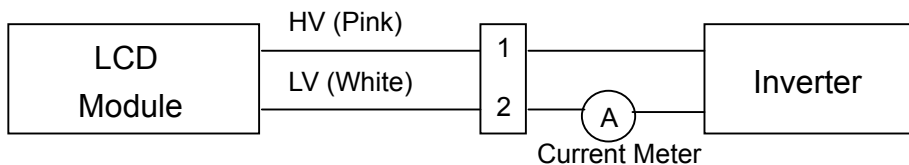


3.2 BACKLIGHT UNIT

 $T_a = 25 \pm 2\text{ }^\circ\text{C}$

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	576	640	704	V_{RMS}	$I_L = 6.0\text{ mA}$
Lamp Current	I_L	3.0	6.0	6.5	mA_{RMS}	(1)
Lamp Turn On Voltage	V_s	-	-	1360 (25 °C)	V_{RMS}	(2)
		-	-	1670 (0 °C)	V_{RMS}	(2)
Operating Frequency	F_L	50	-	80	KHz	(3)
Lamp Life Time	L_{BL}	10,000	-	-	Hrs	(5)
Power Consumption	P_L	-	3.84	-	W	(4), $I_L = 6.0\text{ mA}$

Note (1) Lamp current is measured by utilizing a high frequency current meter as shown below:



Note (2) The voltage shown above should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may generate interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) $P_L = I_L \times V_L$

Note (5) The lifetime of lamp is defined as the time when it continues to operate under the conditions at $T_a = 25 \pm 2 \text{ }^\circ\text{C}$ and $I_L = 6.0 \text{ mA}_{\text{RMS}}$ until one of the following events occurs:

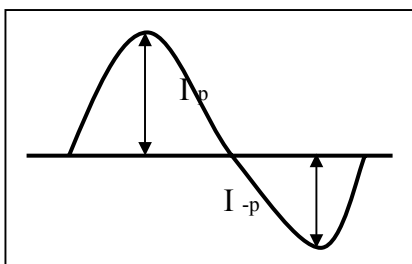
- (a) When the brightness becomes $\leq 50\%$ of its original value.
- (b) When the effective ignition length becomes $\leq 80\%$ of its original value. (Effective ignition length is defined as an area that the brightness is less than 70% compared to the center point.)

Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid generating too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform. (Unsymmetrical ratio is less than 10%) Please do not use the inverter, which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

- a. The asymmetry rate of the inverter waveform should be 10% below;
- b. The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$;
- c. The ideal sine wave form shall be symmetric in positive and negative polarities.



* Asymmetry rate:

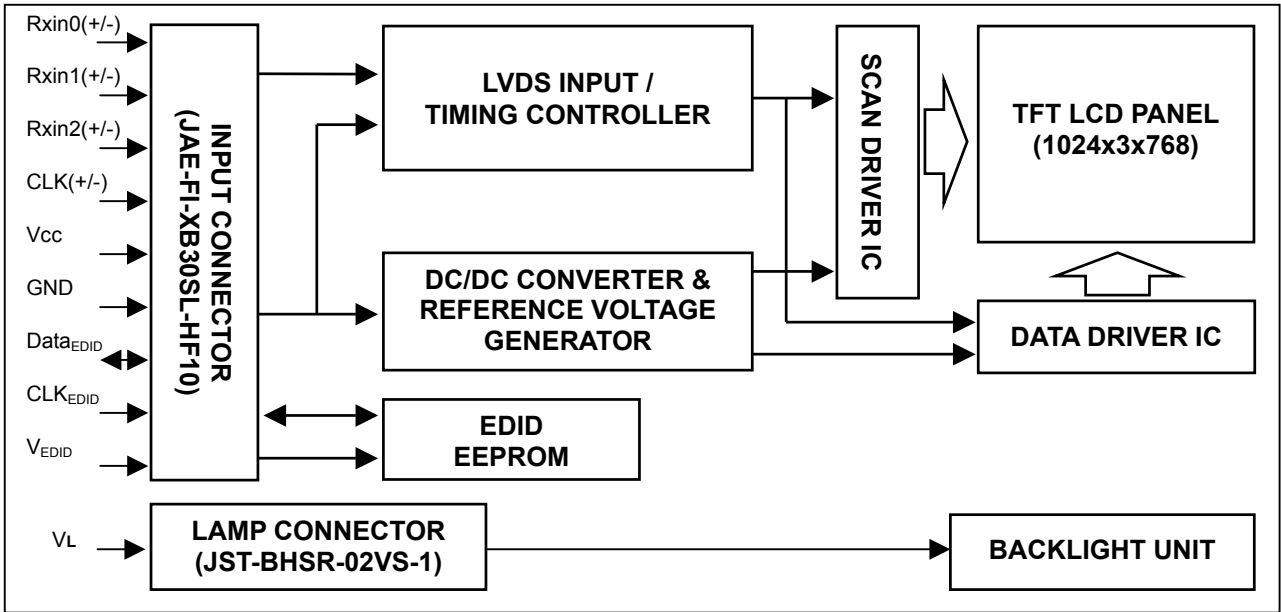
$$| I_p - I_{-p} | / I_{\text{rms}} * 100\%$$

* Distortion rate

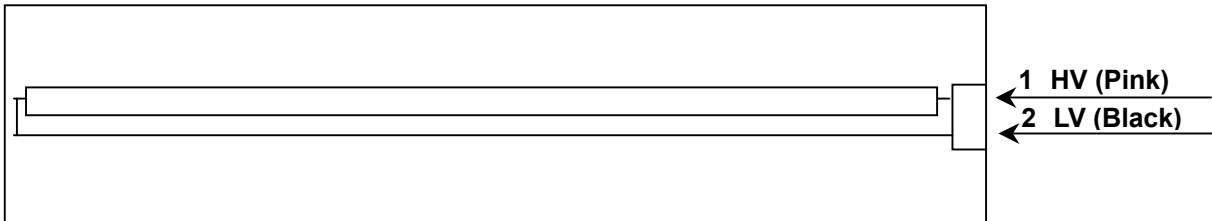
$$I_p \text{ (or } I_{-p}) / I_{\text{rms}}$$

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Vss	Ground		
2	Vcc	Power Supply +3.3 V (typical)		
3	Vcc	Power Supply +3.3 V (typical)		
4	V _{EDID}	DDC 3.3V Power		DDC 3.3V Power
5	Test	Panel Self Test		
6	CLK _{EDID}	DDC Clock		DDC Clock
7	DATA _{EDID}	DDC Data		DDC Data
8	Rxin0-	LVDS Differential Data Input	Negative	R0~R5,G0
9	Rxin0+	LVDS Differential Data Input	Positive	
10	Vss	Ground		G1~G5,B0,B1
11	Rxin1-	LVDS Differential Data Input	Negative	
12	Rxin1+	LVDS Differential Data Input	Positive	
13	Vss	Ground		B2~B5,DE,Hsync,Vsync
14	Rxin2-	LVDS Differential Data Input	Negative	
15	Rxin2+	LVDS Differential Data Input	Positive	
16	Vss	Ground		LVDS Level Clock
17	CLK-	LVDS Clock Data Input	Negative	
18	CLK+	LVDS Clock Data Input	Positive	
19	Vss	Ground		
20	NC	Non-Connection		
21	NC	Non-Connection		
22	Vss	Ground		
23	NC	Non-Connection		
24	NC	Non-Connection		
25	Vss	Ground		
26	NC	Non-Connection		
27	NC	Non-Connection		
28	Vss	Ground		
29	NC	Non-Connection		
30	NC	Non-Connection		

Note (1) Connector Part No.: JAE-FI-XB30SL-HF10 or equivalent

Note (2) User's connector Part No: JAE-FI-X30C2L or equivalent

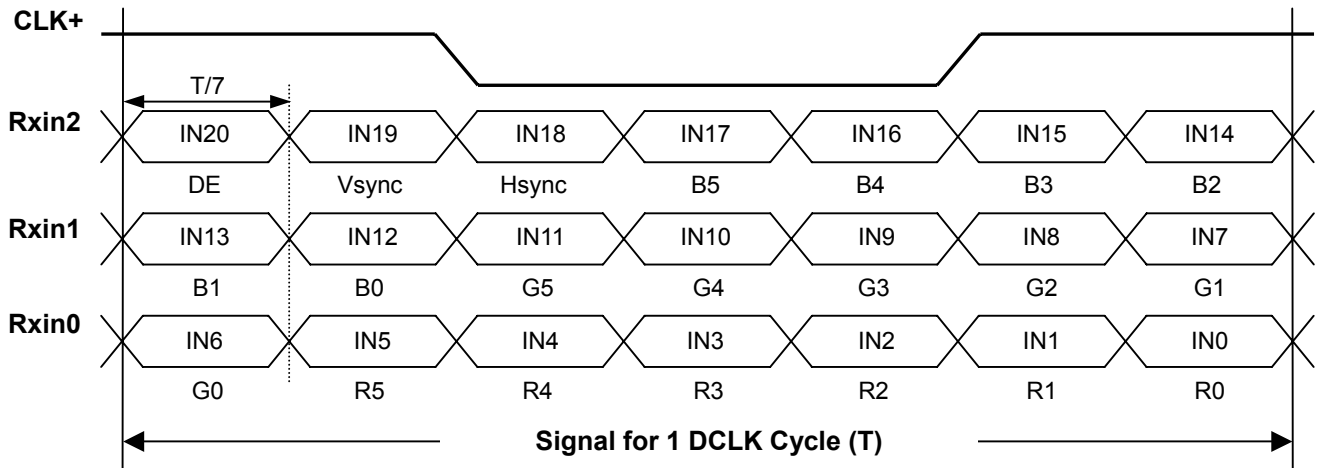
5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Color
1	HV	High Voltage	Pink
2	LV	Ground	Black

Note (1) Connector Part No.: JST-BHSR-02VS-1 or equivalent

Note (2) User's connector Part No.: JST-SM02B-BHSS-1-TB or equivalent

5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL



5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
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	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.5 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPD1 standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name ("CMO")	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AF	10101111
10	0A	ID product code (N141XB)	3F	00111111
11	0B	ID product code (hex LSB first; N141XB)	9C	10011100
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed "14H")	14	00010100
17	11	Year of manufacture (fixed "2004")	0E	00001110
18	12	EDID structure version # ("1")	01	00000001
19	13	EDID revision # ("3")	03	00000011
20	14	Video I/P definition ("digital")	80	10000000
21	15	Max H image size ("28 cm")	1C	00011100
22	16	Max V image size ("21 cm")	15	00010101
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("Active off, RGB Color")	0A	00001010
25	19	Red/Green (Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0)	34	00110100
26	1A	Blue/White (Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0)	85	10000101
27	1B	Red-x (Rx = "0.570")	92	10010010
28	1C	Red-y (Ry = "0.335")	55	01010101
29	1D	Green-x (Gx = "0.325")	53	01010011
30	1E	Green-y (Gy = "0.570")	92	10010010
31	1F	Blue-x (Bx = "0.150")	26	00100110
32	20	Blue-y (By = "0.125")	20	00100000
33	21	White-x (Wx = "0.313")	50	01010000
34	22	White-y (Wy = "0.329")	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2 (1024x768@60Hz)	08	00001000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("63.5MHz", According to VESA CVT Rev1.1)	CE	11001110
55	37	# 1 Pixel clock (hex LSB first)	18	00011000
56	38	# 1 H active ("1024")	00	00000000
57	39	# 1 H blank ("304")	30	00110000
58	3A	# 1 H active : H blank ("1024 : 304")	41	01000001
59	3B	# 1 V active ("768")	00	00000000
60	3C	# 1 V blank ("30")	1E	00011110
61	3D	# 1 V active : V blank ("768 : 30")	30	00110000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("104")	68	01101000
64	40	# 1 V sync offset : V sync pulse width ("3 : 4")	34	00110100
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("24 : 136 : 3 : 4")	00	00000000
66	42	# 1 H image size ("285 mm")	1D	00011101
67	43	# 1 V image size ("214 mm")	D6	11010110
68	44	# 1 H image size : V image size ("285 : 214")	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives, DE only note: LSB is set to "1" if panel is DE-timing only. H/V can be ignored.	19	00011001
72	48	Detailed timing description # 2 Pixel clock ("52 MHz", According to VESA CVT Rev1.1)	50	01010000
73	49	# 2 Pixel clock (hex LSB first)	14	00010100
74	4A	# 2 H active ("1024")	00	00000000
75	4B	# 2 H blank ("288")	20	00100000
76	4C	# 2 H active : H blank ("1024 : 288")	41	01000001
77	4D	# 2 V active ("768")	00	00000000
78	4E	# 2 V blank ("25")	19	00011001
79	4F	# 2 V active : V blank ("768 : 38")	30	00110000
80	50	# 2 H sync offset ("40")	28	00101000
81	51	# 2 H sync pulse width ("104")	68	01101000
82	52	# 2 V sync offset : V sync pulse width ("3 : 4")	34	00110100
83	53	# 2 H sync offset : H sync pulse width : V sync offset : V sync width ("24 : 136 : 3 : 4")	00	00000000

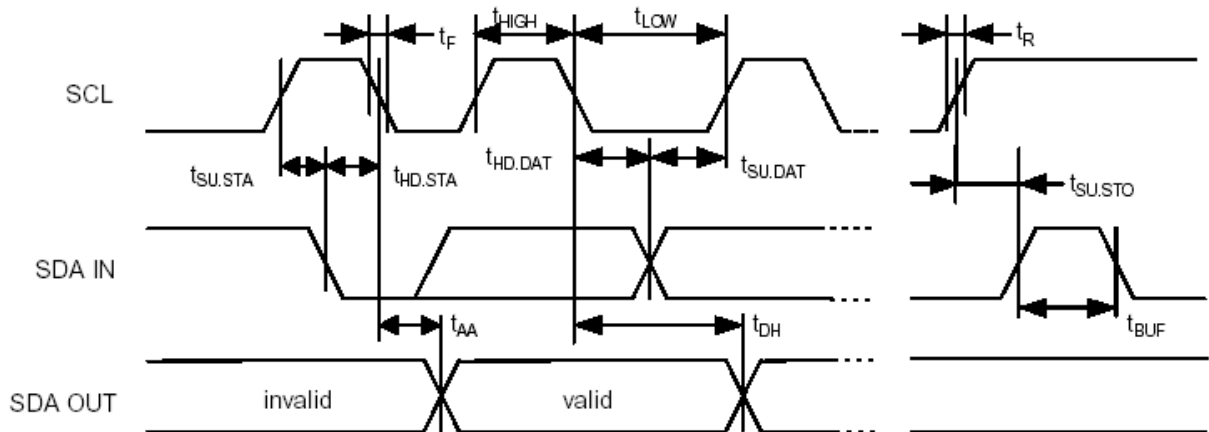
Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
84	54	# 2 H image size ("285 mm")	1D	00011101
85	55	# 2 V image size ("214 mm")	D6	11010110
86	56	# 2 H image size : V image size ("285 : 214")	10	00010000
87	57	# 2 H boarder ("0")	00	00000000
88	58	# 2 V boarder ("0")	00	00000000
89	59	Module "A" Revision = Example: 00, 01, 02, 03, etc.	00	00000000
90	5A	Detailed timing description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 FE (hex) defines ASCII string (Model Name "N141XB", ASCII)	FE	11111110
94	5E	# 3 Flag	00	00000000
95	5F	# Dell P/N "N5015" 1st character ("N")	4E	01001110
96	60	# Dell P/N " N5015" 1st character ("5")	35	00110101
97	61	# Dell P/N " N5015" 1st character ("0")	30	00110000
98	62	# Dell P/N " N5015" 1st character ("1")	31	00110001
99	63	# Dell P/N " N5015" 1st character ("5")	35	00110101
100	64	LCD Supplier EEDID Revision #: "2"	32	00110010
101	65	Manufacturer P/N ("N")	4E	01001110
102	66	Manufacturer P/N ("1")	31	00110001
103	67	Manufacturer P/N ("4")	34	00110100
104	68	Manufacturer P/N ("1")	31	00110001
105	69	Manufacturer P/N ("X")	58	01011000
106	6A	Manufacturer P/N ("B")	42	01000010
107	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000
110	6E	Flag	00	00000000
111	6F	Data Type Tag:	FE	11111110
112	70	Flag	00	00000000
113	71	SMBUS value @ 10 [cd/m2]=	FF	11111111
114	72	SMBUS value @ 17 [cd/m2]=	E5	11100101
115	73	SMBUS value @ 23 [cd/m2]=	D4	11010100
116	74	SMBUS value @ 30 [cd/m2]=	C5	11000101
117	75	SMBUS value @ 60 [cd/m2]=	9A	10011010
118	76	SMBUS value @ 110 [cd/m2]=	67	01100111
119	77	SMBUS value @ 150 [cd/m2]=	3B	00111011
120	78	SMBUS value @ max [cd/m2]=	00	00000000
121	79	Numbers of LVDS Recevier chip = 1	01	00000001
122	7A	BIST Enable: Yes = '01' No = '00' ("Yes")	01	00000001
123	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
124	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
125	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000

126	7E	Extension flag	00	00000000
127	7F	Checksum	59	01011001

5.6 EDID SIGNAL SPECIFICATION

(1) EDID Power

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc	Read Operation	2.2	—	5.5	V



(2) DC characteristics

		Symbol	Min.	Max.	Unit	Index
SCL, SDA terminal input voltage	High Voltage	V _{IH}	0.7×V _{CC}	—	V	
	Low Voltage	V _{IL}	—	0.3×V _{CC}	V	
Hysteresis Voltage		V _{HYS}	0.05 V _{CC}	—	V	
Output Voltage		V _{OL1} V _{OL2}	—	0.4 0.6	V	I _{OL} =3mA, C _C =2.5V I _{OL} =6mA, C _C =2.5V
Input Leak current (V _{in} =0.1V~V _{CC})		I _{LI}	-10 -10	10 50	uA	WP=V _{SS} WP=V _{CC}
Output Leak current		I _{LO}	-10	10	uA	V _{out} =0.1V~V _{CC} , WP=V _{SS}
Terminal capacity(Input, Output)		C _{in} , C _{out}	—	10	pF	V _{CC} =5.0V T _a =25 ⁰ C, F _{clk} =1.0MHz
Operating current		ICC Write ICC Read	—	3 1	mA	V _{CC} =5.5V, SCL=400KHz
Stillness current (SDA=SCL=V _{CC}) (WP=V _{SS} ,A0,A1,A2=V _{SS})		ICCS	—	30 100	uA	V _{CC} =3.0V V _{CC} =5.5V

(3) AC characteristics (VCC=2.5~5.5V standard operation mode)

Item	Symbol	VCC=2.5V-5.5V (Standard operation mode)		VCC=4.5V-5.5V (High-speed operation mode)		Unit	Index
		Min.	Max.	Min.	Max.		
Clock frequency	Fclk	—	100	—	400	KHz	
Clock High Time	THIGH	4000	—	900	—	ns	
Clock Low Time	TLOW	4700	—	1300	—	ns	
SDA, SCL falling time	TR	—	1000	—	300	ns	
SDA, SCL rising time	TF	—	300	—	300	ns	
START hold time	THD: STA	4000	—	600	—	ns	
START setup time	TSU: STA	4700	—	600	—	ns	
Data input hold time	THD: Data	0	—	0	—	ns	
Data input setup time	TSU: Data	250	—	100	—	ns	
STOP setup time	TSU: STO	4700	—	600	—	ns	
Output decision time from a clock	TAA	—	3500	100	900	ns	
Bus free time	TBUF	4700	—	1300	—	ns	
Rising time of Min VIH, VIL	TOF	—	250	20	250	ns	CB ≤ 100pF
Spike oppression	TSP	—	50	—	50	ns	
A write-in cycle time	TWR	—	10	—	10	ms	Byte and page mode
The number of times of data rewriting	—	1M	—	1M	—	cycles	VCC=5.0V Ta=25°C,

6. INVERTER SPECIFICATION

6.1 Connector type:

Input connector type: **LVC-D20SFYG (HONDA)**

Output connector: **JST SM02B-BHSS-1-TB (JST)**

6.2 Input Connector pin assignment:

Input connector		Comments
HONDA	LVC-D20SFYG	
Pin	Function	
1	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
2	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
3	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
4	NC	No Connection
5	GND	Ground
6	5VSUS	This should be used as power source for the control circuitry on the inverter
7	5VALW	This should be used as power source that stores the brightness/contrast values & the circuit that interfaces with SMB_CLK & SMB_DAT
8	GND	Ground
9	SMB_DAT	SMBus interface for sending brightness & contrast information to the inverter/panel
10	SMB_CLK	SMBus interface for sending brightness & contrast information to the inverter/panel
11	GND	Ground
12	FPBACK	Control signal input into the inverter to turn the backlight ON & OFF (1 - ON, 0 - OFF)
13	GND	Ground
14	LAMP_STAT	Lamp status (Feedback, Lamp On = 5v, Lamp Off 0v), from control chip
15 ~ 20	NC	No Connection

Absolute maximum ratings

Items	Absolute max. ratings	Unit
INV_SRC (Voltage)	-1.0~23.5	V
FPBACK/SMB_CLK/SMB_DAT (Voltage)	-1.0~5.5	V

6.3 Output connector pin assignment

Pin	Name	Description
1	CFL-High	High-voltage output to the CCFL
2	CFL-Low	Low-voltage output to the CCFL

Absolute maximum ratings

Items	Absolute max. ratings	Unit
INV_SRC (Voltage)	-1.0~23.5	V
FPBACK/SMB_CLK/SMB_DAT (Voltage)	-1.0~5.5	V

6.4 General electrical specification:

Electrical characteristics:

No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Input Voltage	INV_SRC		7.5	14.4	21	V
2	Input Signal Level for 5VSUS	5VSUS		4.85	5	5.2	V
3	Input Signal Level for 5VALW	5VALW		4.85	5	5.2	V
4	Input Power	Pin(Max)	Vin=7.5V~21V SMB_DAT=00H	-	-	5.7	W
5	Backlight ON/OFF Control	FPBACK=ON	Enable the inverter	2.0	-	5.25	V
		FPBACK=OFF	Disable the inverter	-0.3	-	0.8	V
6	Brightness Adjust (Lamp Current Control)	SMB_DAT	Control by SMBus	FFH	-	00H	-
7	Output Voltage	Vout	IL = 6.0mA(typ)	TBD	640	TBD	Vrms
8	Output Current	Iout (Min)	Vin=7.5V~21V SMB_DAT=FFH Ta=25°C, after running 30 min.	2.0	TBD	TBD	mArms
		Iout (Max)	Vin=7.5V~21V SMB_DAT=00H Ta=25°C, after running 30 min.	5.7	6.0	6.3	mArms
9	Operation Frequency	Freq	Vin=7.5V~21V	(45)	-	(65)	KHz

10	Burst mode frequency	f_B	$V_{in}=7.5V\sim 21V$	200	-	220	Hz
11	Open Lamp Voltage	V_{open}	No Load	(1400)	(1670)	(1800)	V_{rms}
12	Striking Time	T_s	No Load	0.6	1	1.4	Sec
13	Efficiency	η	$V_{in}=7.5V$, SMB_DAT=00H (RES LOAD=100K ohm)	(80)	-	-	%
14	Start and Delay Time		$V_{in}=14.4V$, SMB DAT=FFH	-	130	200	μS
15	Start -up time			-	-	0.1	Sec

- Input Voltage

The operating input voltage of inverter shall be defined.

The inverter shall ignite the CCFL lamp at minimum input voltage at any environment conditions.

- On/Off control

Enable: At “ON” condition (FPBACK=Hi), enable the inverter.

Disable: At “OFF” condition (FPBACK=Lo), disable the inverter.

- Quiescent current

At the inverter “OFF” condition, input quiescent should be less than 0.1mA.

- Open lamp voltage

The inverter start-up output voltage will be above “ V_{open} ” for “ T_s ” minimum at any condition under specify until lamp to be ignited. The inverter should be shutdown if lamp ignition was failed in “ T_s ” maximum. The inverter shall be capable of withstanding the output connections open without component over-stress / fire / smoke /arc.

- Burst mode frequency

The burst mode frequency should be in specification in any environment condition and electrical condition.

- Brightness control

SM-BUS values for panel luminance are to be included in the on LCD board EEDID ROM chip table. The supplier will measure panel luminance in a system and define the SMBUS values for each of the 8 required luminance levels. The panel luminance, for which SMBUS values will be provided in the EEDID from byte # 113(hex #71), to byte # 120, (hex # 78), is show in the table below. The inverter supplier should provide these appropriate values to CMO.

Step Count	Step 1	Step 2	Step3	Step 4	Step 5	Step 6	Step 7	Step 8
Address	Byte 113	Byte 114	Byte 115	Byte 116	Byte 117	Byte 118	Byte 119	Byte 120
SM-Bus Data Value	FF	E5	D4	C5	9A	67	3B	00
Luminance (nits)	10	17	23	30	60	110	150	Max

- Output ripple ratio

$$\text{Ripple ratio} = 2 * (\text{Ipeak} - \text{Ivalley}) / (\text{Ipeak} + \text{Ivalley}) * 100\%$$

The Ripple ratio should be less than 5% and ripple frequency should be less than 200 Hz.

- Power up Overshoot & Undershoot

Overshoot & Undershoot at power up should not exceed the following limits.

Vin	Output current Io(rms)	Io (dI) Overshoot/Undershoot	Settling time (dT)
0→Vin(min.)	Io(max.)	150% / 50%	5 ms max.
	Io(min.)		
0→Vin(typ.)	Io(max.)	150% / 50%	5 ms max.
	Io(min.)		
0→Vin(max.)	Io(max.)	150% / 50%	5 ms max.
	Io(min.)		

$$dI = I_{\text{max.}} - I_o \quad \text{or} \quad dI = (I_o - I_{\text{min.}}) / I_o$$

- Output connections short protection

The inverter shall be capable of withstanding the output connections short without damage or over-stress. And the inverter maximum input power shall be limited within 1W.

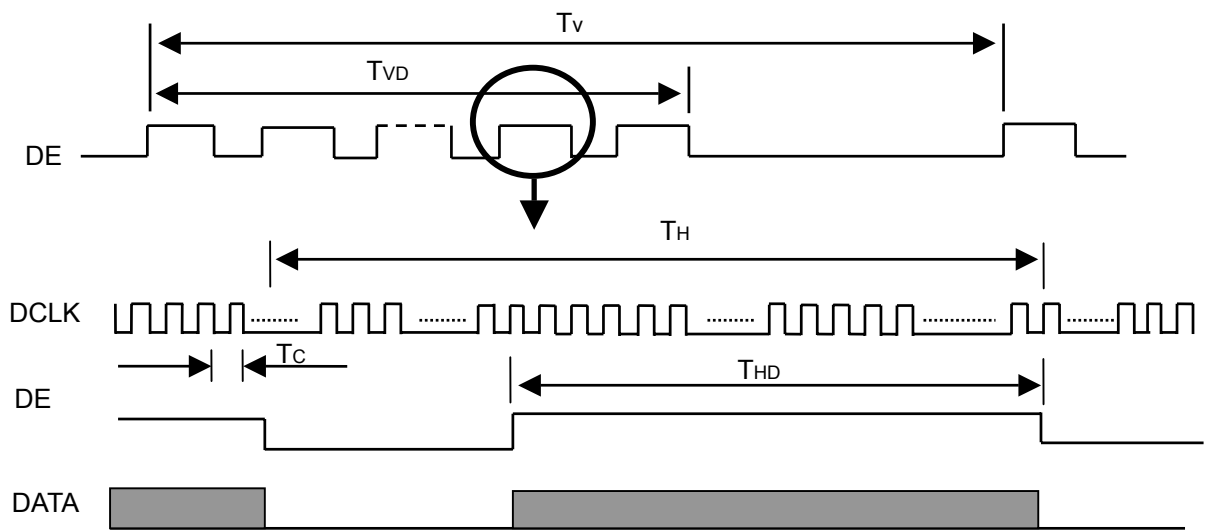
7. INTERFACE TIMING

7.1 INPUT SIGNAL TIMING SPECIFICATIONS

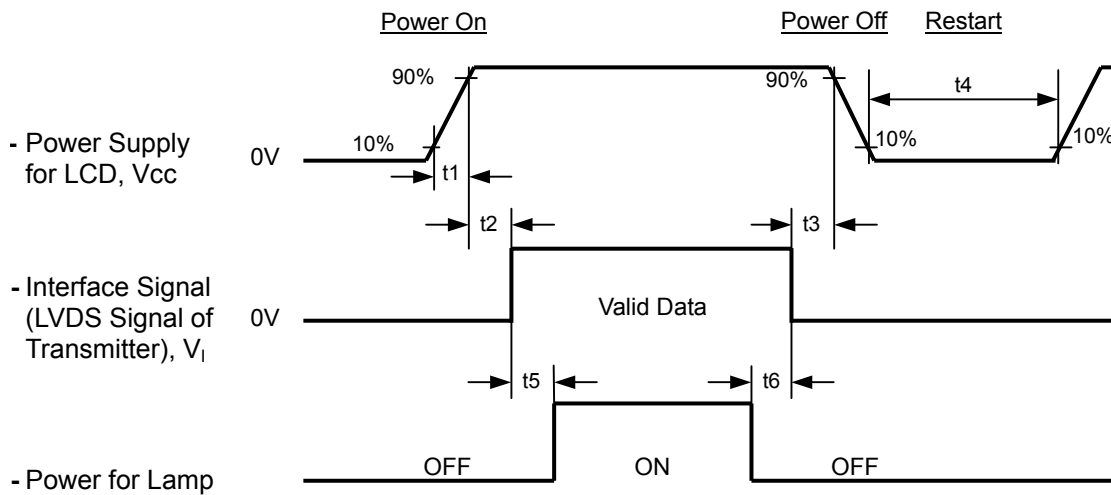
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	50	65	68	MHz	-
DE	Vertical Total Time	Tv	771	806	850	TH	-
	Vertical Addressing Time	TvD	768	768	768	TH	-
	Horizontal Total Time	TH	1200	1344	1500	Tc	-
	Horizontal Addressing Time	THD	1024	1024	1024	Tc	-

INPUT SIGNAL TIMING DIAGRAM



7.2 POWER ON/OFF SEQUENCE



Timing Specifications:

$$470\mu\text{s} \leq t1 \leq 10 \text{ msec}$$

$$0 < t2 \leq 50 \text{ msec}$$

$$0 < t3 \leq 50 \text{ msec}$$

$$t4 \geq 500 \text{ msec}$$

$$t5 \geq 200 \text{ msec}$$

$$t6 \geq 200 \text{ msec}$$

Note (1) Please avoid floating state of interface signal at invalid period.

Note (2) When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

8. OPTICAL CHARACTERISTICS

8.1 TEST CONDITIONS

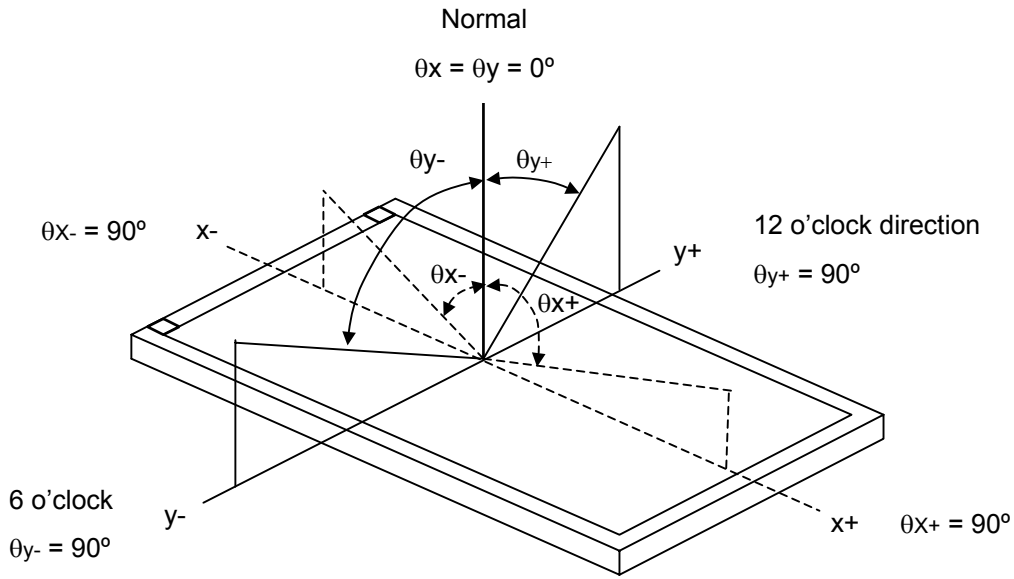
Item	Symbol	Value	Unit
Ambient Temperature	T _a	25±2	°C
Ambient Humidity	H _a	50±10	%RH
Supply Voltage	V _{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I _L	6.0	mA
Inverter Driving Frequency	F _L	55	KHz
Inverter	Sumida- IV11145/T-LF or Delta- DAC-07B046		

The measurement methods of optical characteristics are shown in Section 7.2. The following items should be measured under the test conditions described in Section 7.1 and stable environment shown in Note (6).

8.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note		
Contrast Ratio		CR	θ _x =0°, θ _y =0° Viewing Normal Angle	300	-	-	-	(2), (6)		
Response Time		T _R		-	6	10	ms	(3)		
		T _F		-	17	25	ms			
Average Luminance of White		L _{AVE}		150	185	-	cd/m ²	(4), (6)		
White Variation of 5 Points		δW _{5p}		80	-	-	%	(6), (7)		
White Variation of 13 Points		δW _{13p}		65	-	-	&	(6), (7)		
Cross Talk		CT		-	-	4.0	%	(5), (6)		
Color Chromaticity	Red	R _x		Viewing Normal Angle	Typ. -0.03	0.570	Typ. +0.03	-	(1), (6)	
		R _y				0.335		-		
	Green	G _x				0.325		-		
		G _y	0.570			-				
	Blue	B _x	0.150			-				
		B _y	0.125			-				
	White	W _x	0.283			0.313		0.343		-
		W _y	0.299			0.329		0.359		-
Color Gamut		C.G%	42	-	-	%	(8)			
Viewing Angle	Horizontal	θ _{x+}	CR≥10	40	45	-	Deg.	(1), (6)		
		θ _{x-}		40	45	-				
	Vertical	θ _{y+}		10	15	-				
		θ _{y-}		30	35	-				

Note (1) Definition of Viewing Angle (θ_x, θ_y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

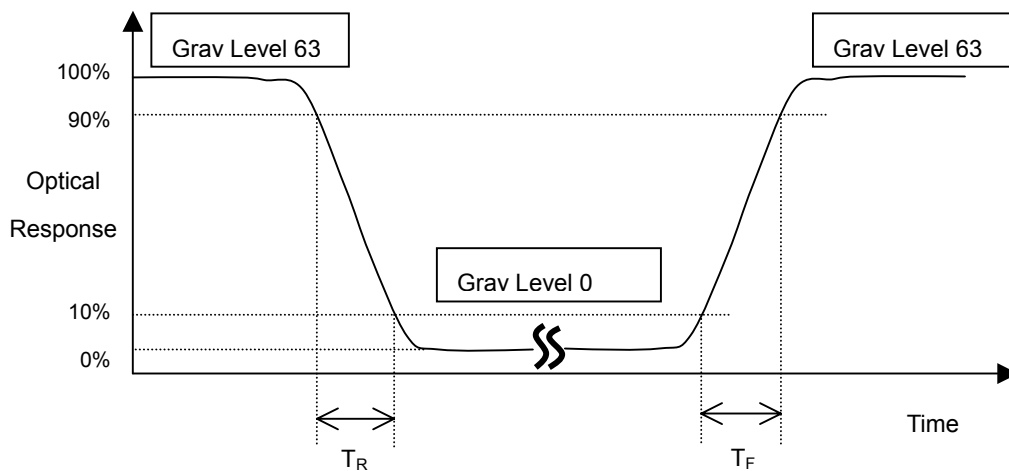
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

$$\text{CR} = \text{CR} (5)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (7).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

Measure the luminance of gray level 63 at 5 points

$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (7).

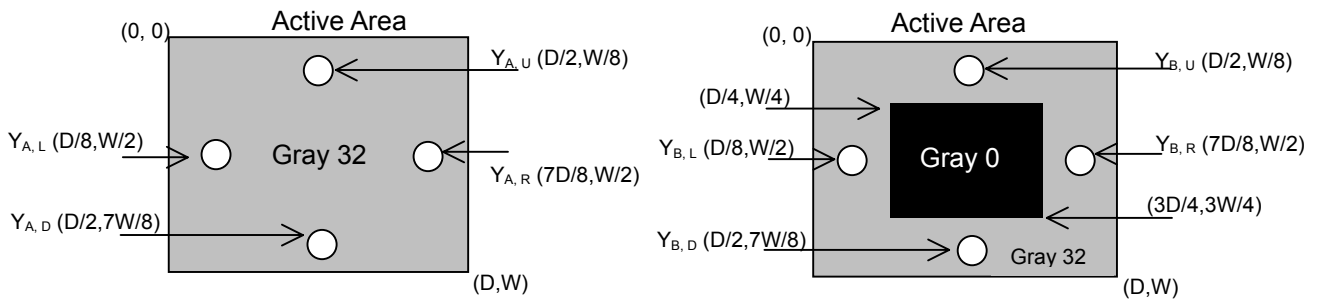
Note (5) Definition of Cross Talk (CT):

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

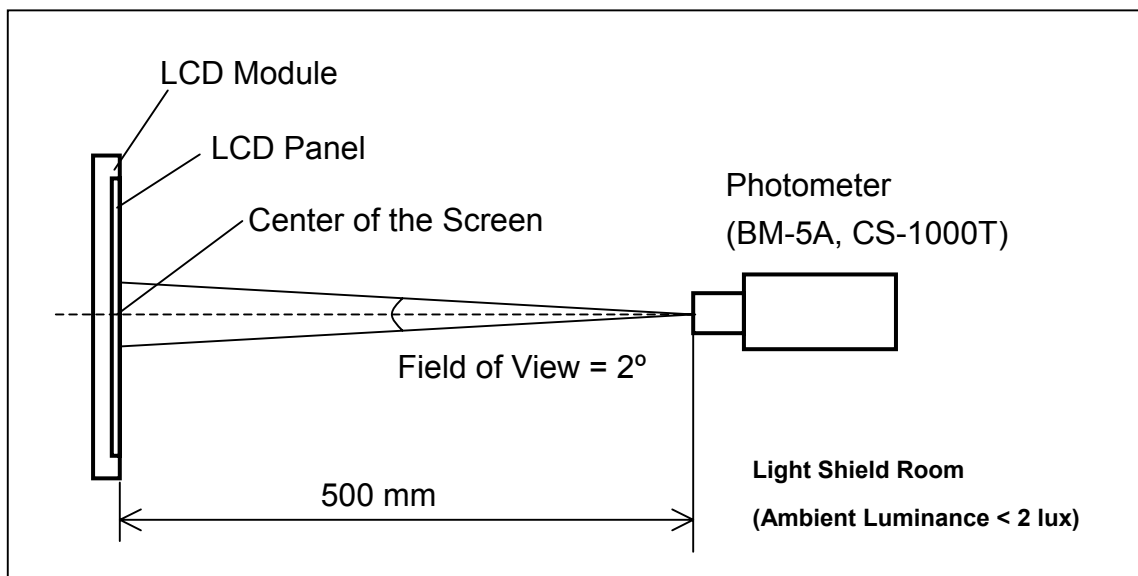
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



Note (6) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

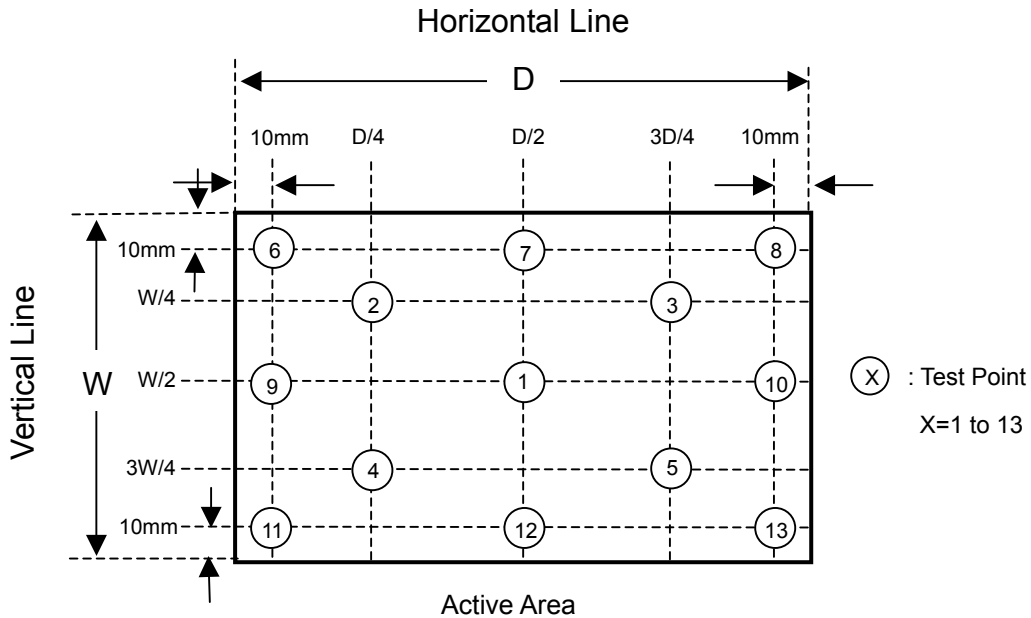


Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 13 points

$$\delta W_{5p} = \text{Minimum [L (1), L (2), L (3), L (4), L (5)]} / \text{Maximum [L (1), L (2), L (3), L (4), L (5)]}$$

$$\delta W_{13p} = \text{Minimum [L (1) ~ L (13)]} / \text{Maximum [L (1) ~ L (13)]}$$



Note (8) Definition of color gamut (C.G%):

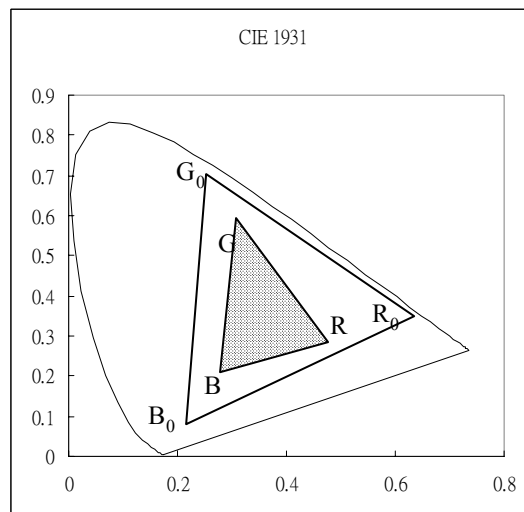
$$C.G\% = \Delta R G B / \Delta R_0 G_0 B_0 \cdot 100\%$$

R_0, G_0, B_0 : color coordinates of red, green, and blue defined by NTSC, respectively.

R, G, B : color coordinates of module on 63 gray levels of red, green, and blue, respectively.

$\Delta R_0 G_0 B_0$: area of triangle defined by R_0, G_0, B_0

$\Delta R G B$: area of triangle defined by R, G, B



9. PRECAUTIONS

9.1 HANDLING PRECAUTIONS

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the lamp wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.

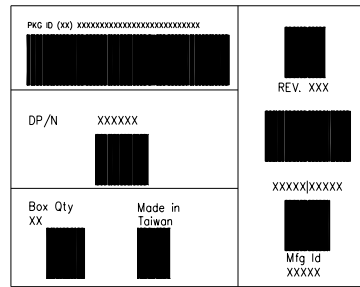
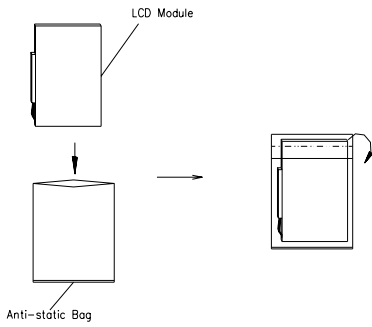
9.2 STORAGE PRECAUTIONS

- (1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (3) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

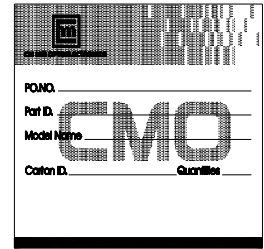
9.3 OPERATION PRECAUTIONS

- (1) Do not pull the I/F connector in or out while the module is operating.
- (2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.
- (3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

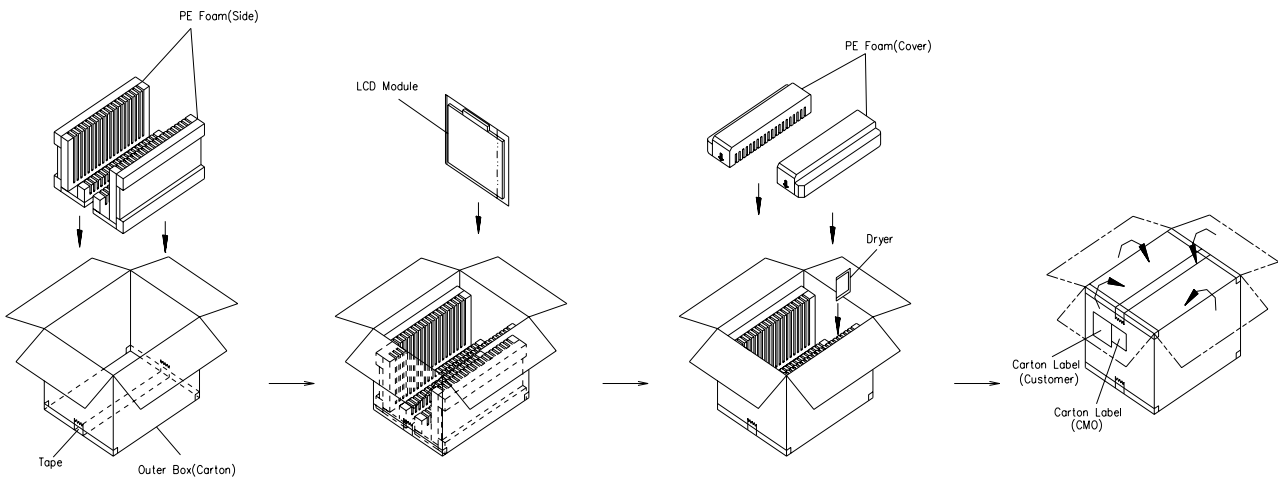
10. PACKING
10.1 CARTON



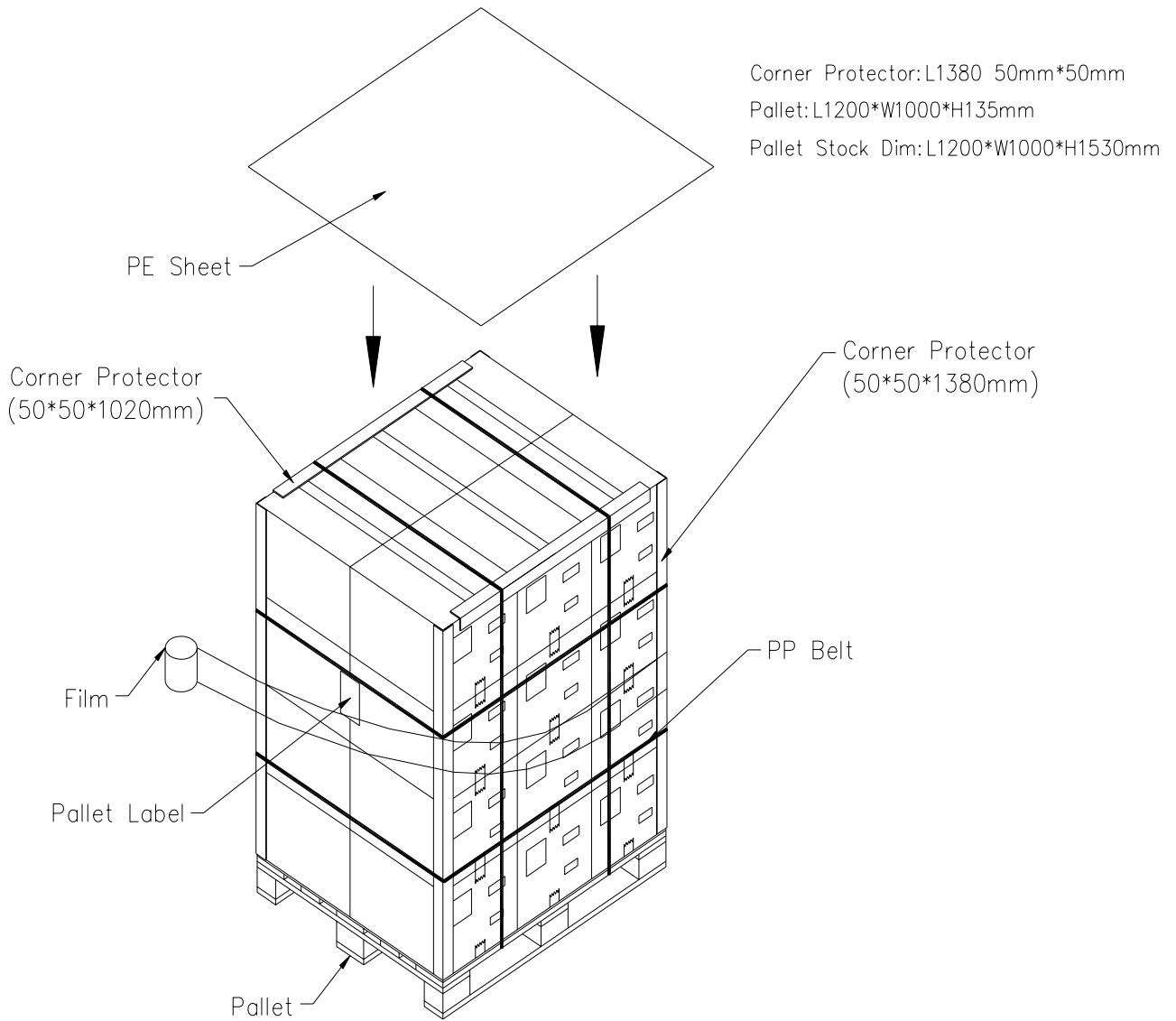
VIEW Carton Label(Customer)



VIEW Carton Label(CMO)

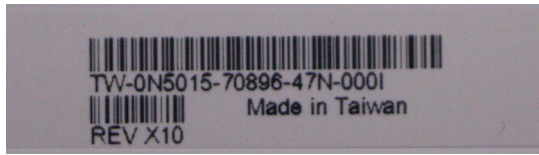


10.2 PALLET



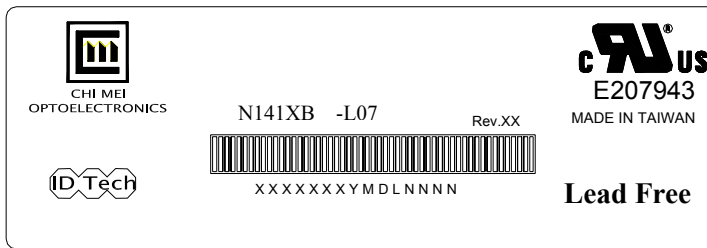
11. DEFINITION OF LABELS

11.1 CUSTOMER MODULE LABEL (ex.)

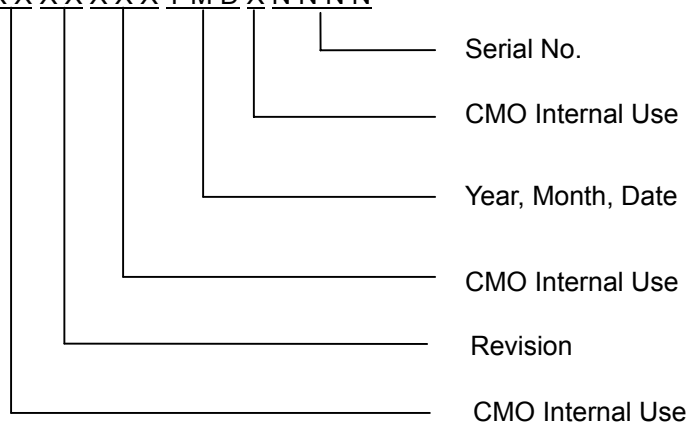


11.2 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: N141XB - L07
- (b) Revision: Rev. XX, for example: C1, C2 ...etc.
- (c) Serial ID: X X X X X X X Y M D X N N N N



Serial ID includes the information as below:

- (a) Manufactured Date: Year: 1~9, for 2001~2009
 Month: 1~9, A~C, for Jan. ~ Dec.
 Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U
- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product

